

PROJECT NAME : HarryPotter 15" EPV51  
PCB NO : LA-G076P

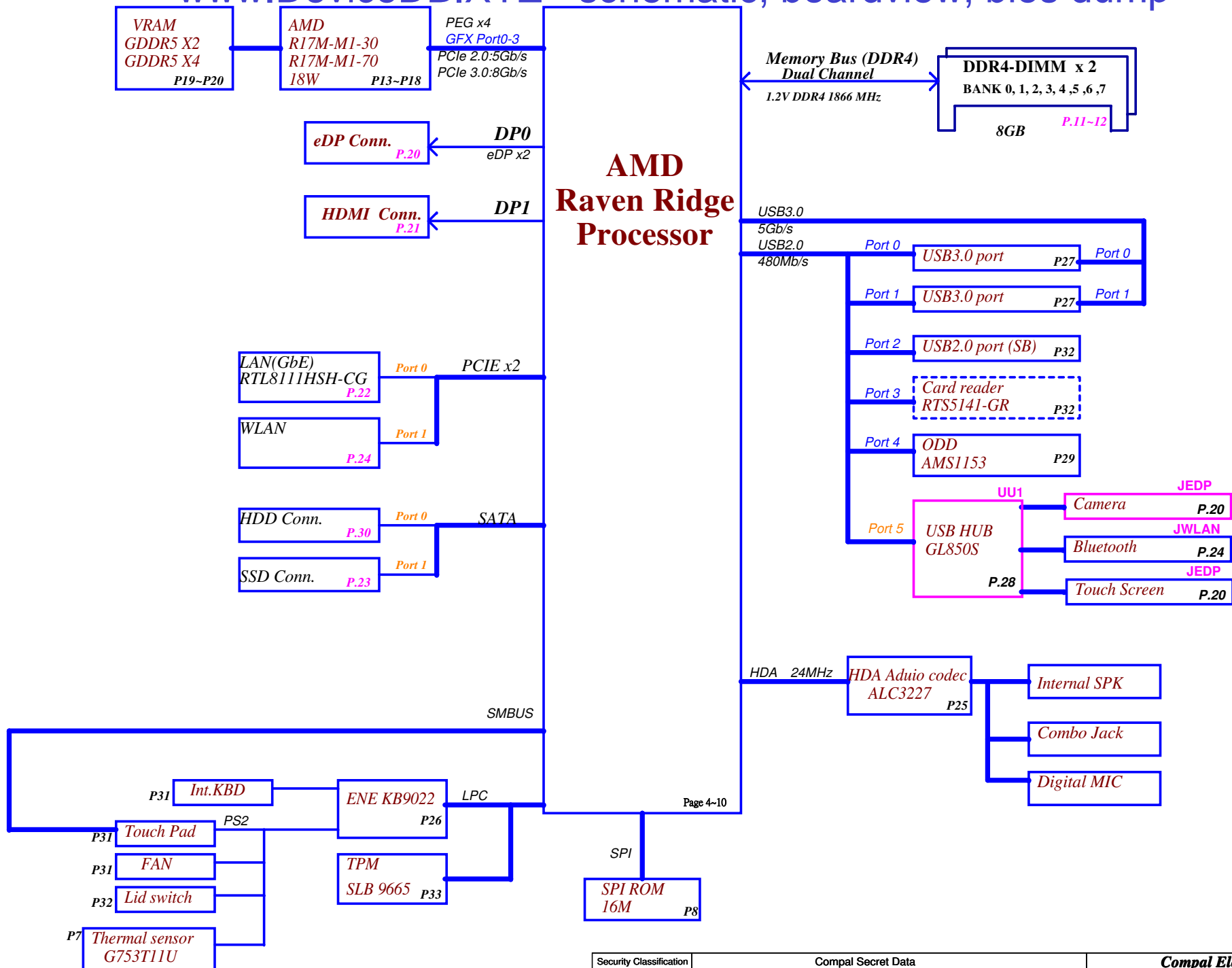
# Compal Confidential

## Schematic Document

AMD Raven Ridge  
AMD R17M-M1-30/R17M-M1-70

2017/09/14  
Rev: 0.1

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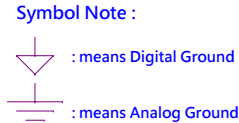


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			Sheet	2	of 50			

@ is NO SMT part (empty)  
short@ : short pad , don't pop.  
@EMI@,@ESD@,@RF@ : Reserve , don't pop.  
RF@ : RF team request, must add.  
EMI@ : EMI team request, must add.  
ESD@ : ESD team request, must add.  
LVDS@ : Support LVDS panel.  
eDP@ : Support eDP panel.  
PX@ : GPU BOM config.

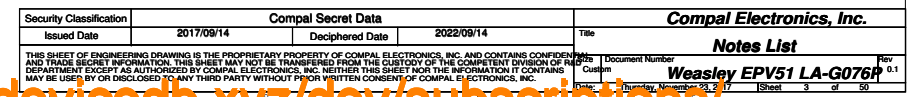
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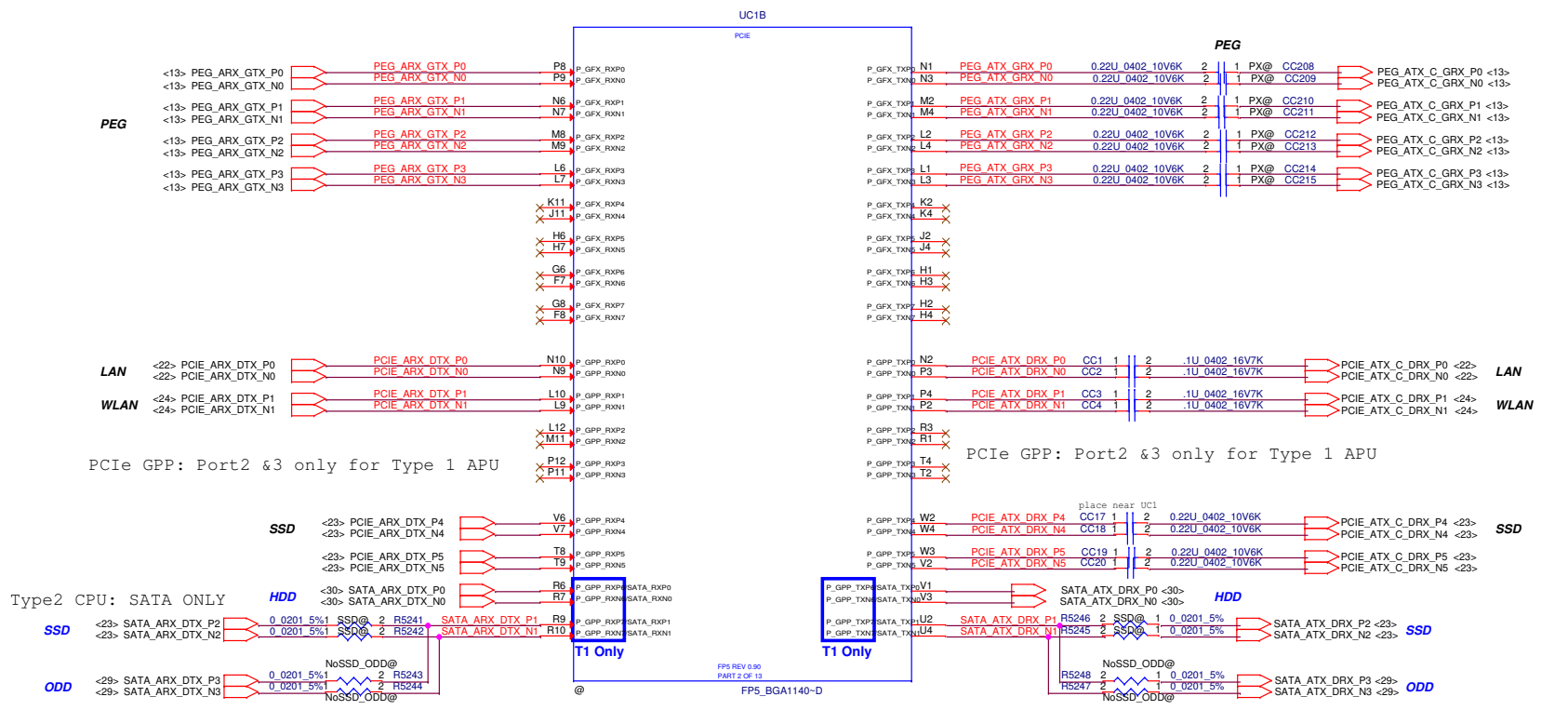
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0 - 0	0 - 0	USB3 Type A
0 - 1	0 - 1	USB3 Type A
0 - 2	0 - 2	USB2 Type A
0 - 3	0 - 3	Card Reader
1 - 0 T1 only	1 - 0	USB-to-SATA (ODD)
	1 - 1	USB HUB



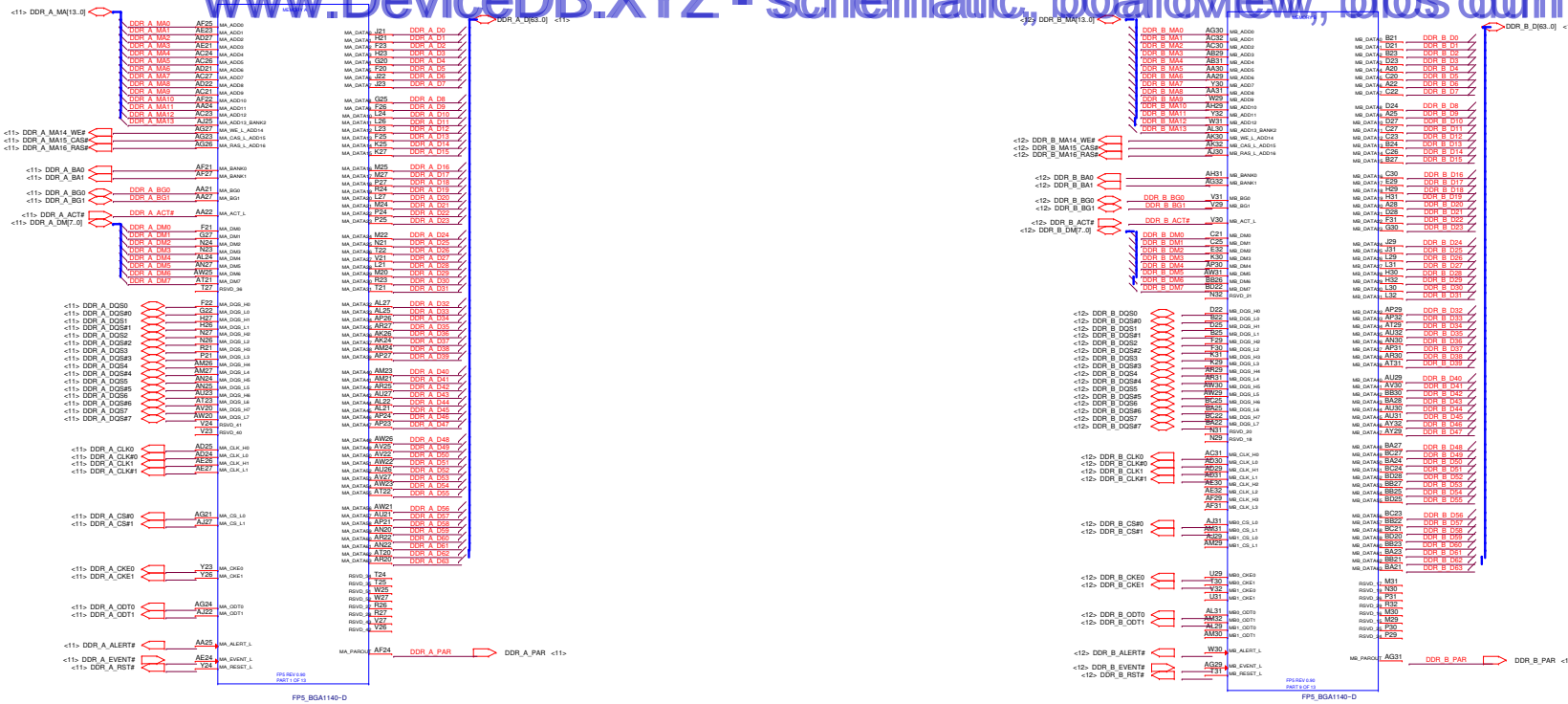
<PCI-E,SATA,CLK>

	PCI-E	SATA	DESTINATION	CLK
	0		LAN	CLK1
	1		WLAN	CLK2
T1 only	2		X	
T1 only	3		X	
	4		PCI-E SSD	CLK3
	5		PCI-E SSD	CLK3
T2 SATA only	6	0	HDD	
T2 SATA only	7	1	SSD or ODD	
GFX			GPU	CLK0



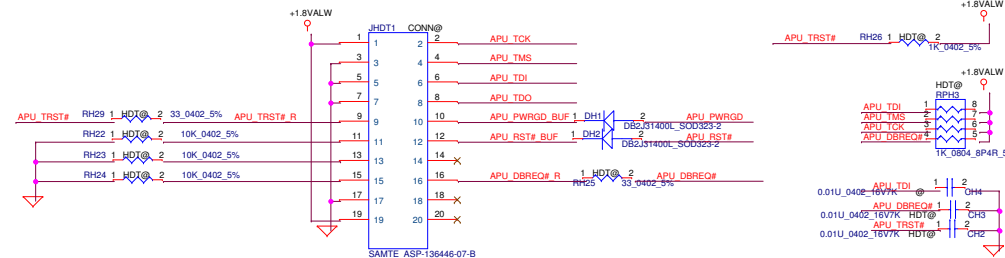
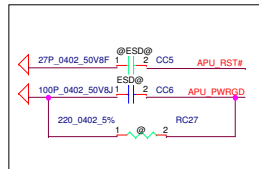
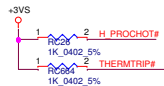
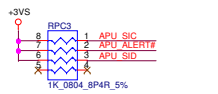
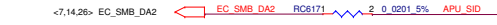
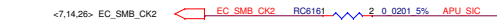
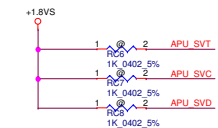
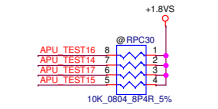
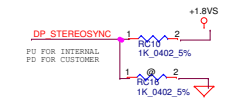
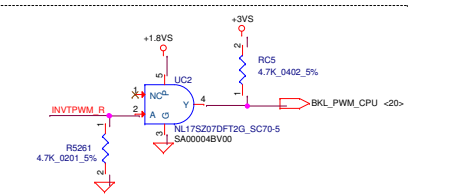
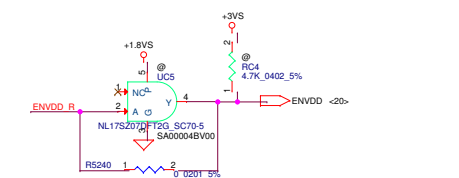


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EVENT# pull high





**Can Place in  $H=0$**

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			Revision	Wesley Spivak LA-G076P 0.1
			Model Number	EP5V1 LA-G076P



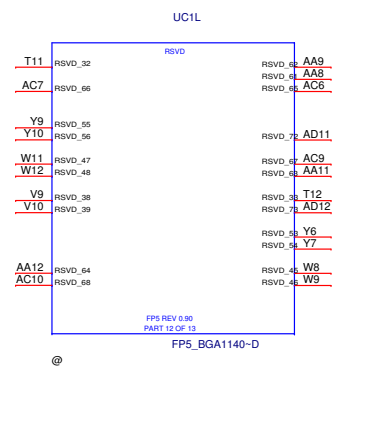
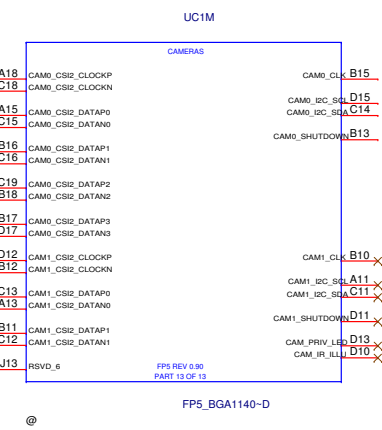
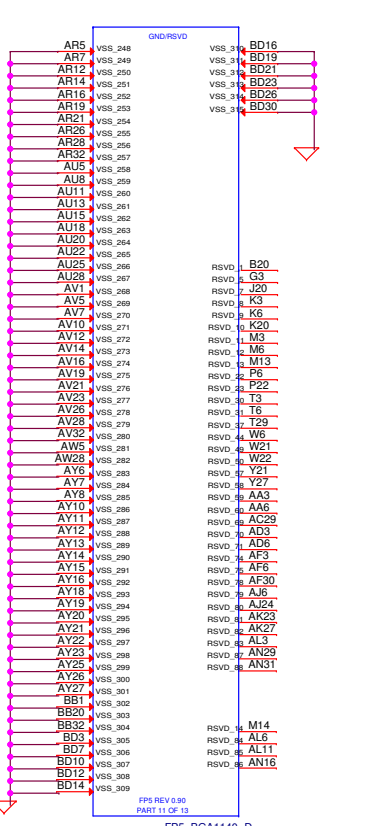
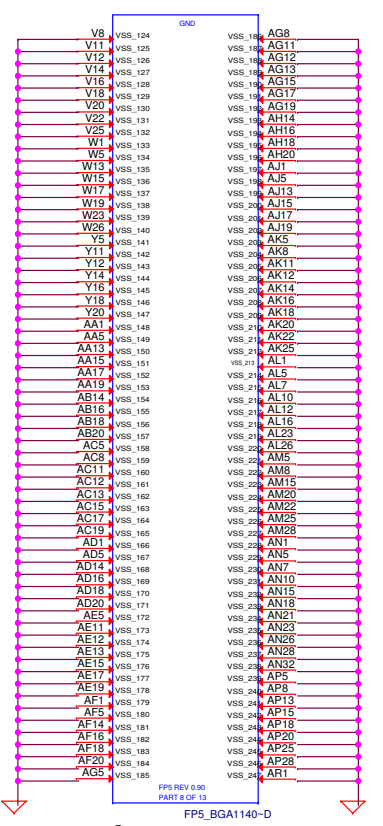
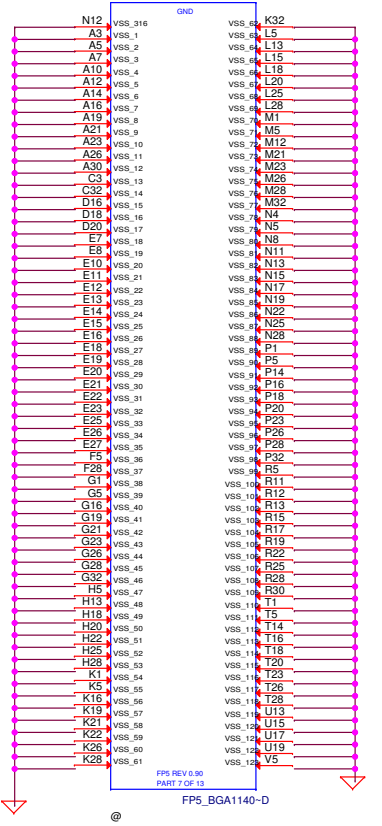




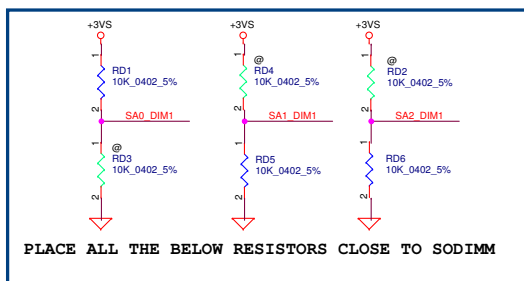
UC1G

UC1H

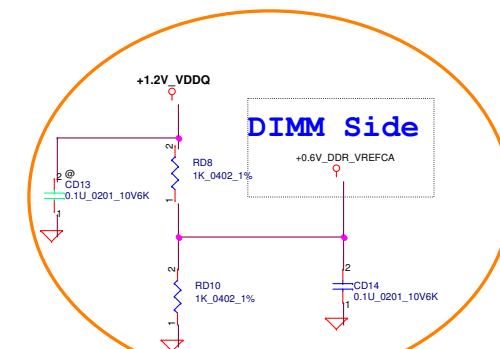
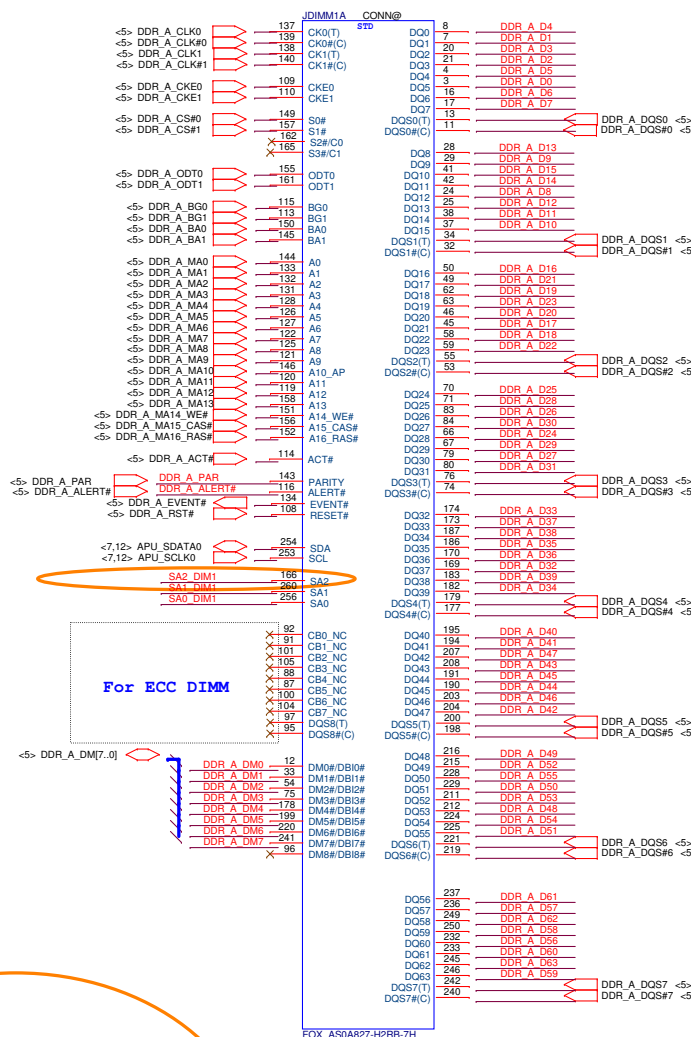
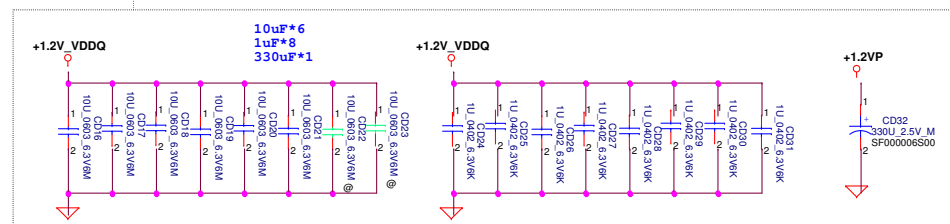
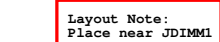
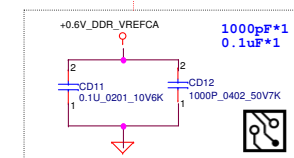
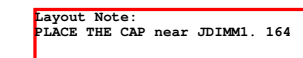
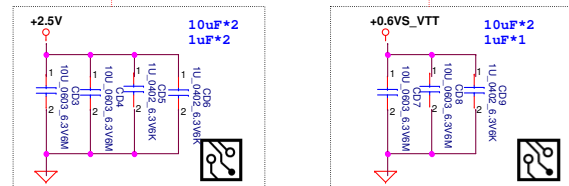
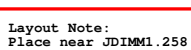
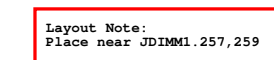
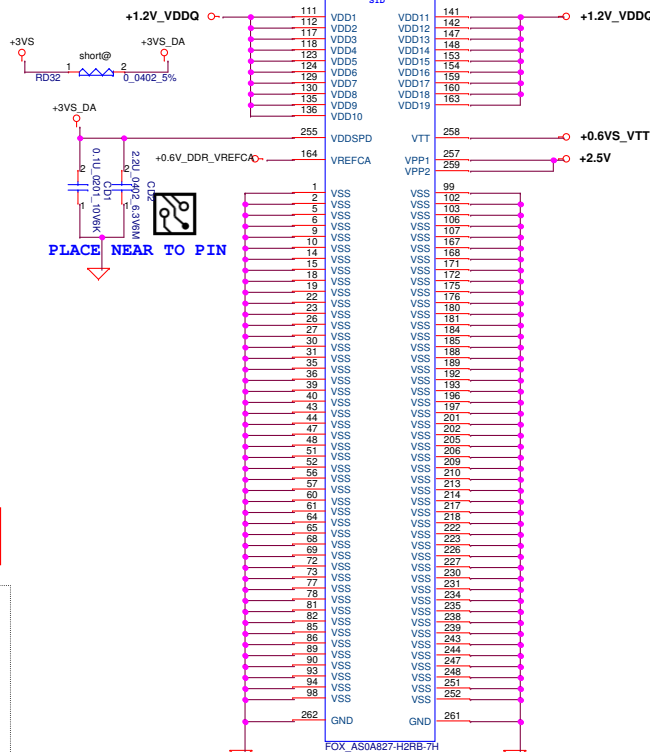
UC1K



Bristol CH-A  
JDIMM1



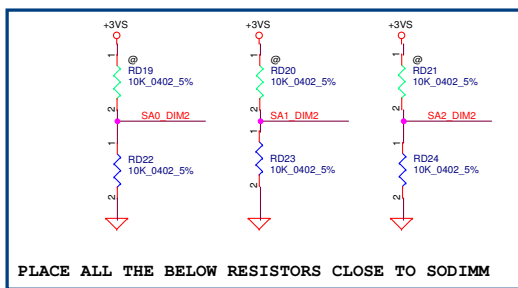
SPD ADDRESS FOR CHANNEL A :  
SA0 = 1; SA1 = 0; SA2 = 0.



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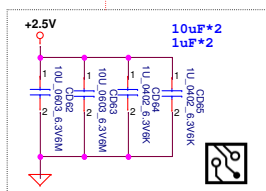
# Bristol CH-B STD

## JDIMM2

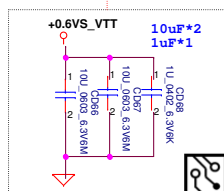


SPD ADDRESS FOR CHANNEL B :  
SA0 = 0; SA1 = 0; SA2 = 0.

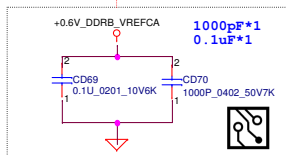
Layout Note:  
Place near JDIMM2.257,259



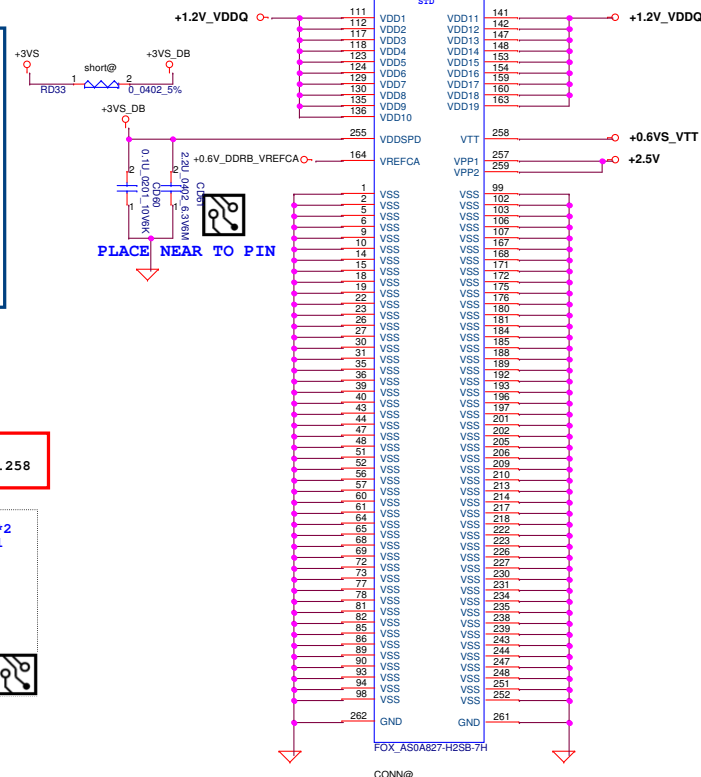
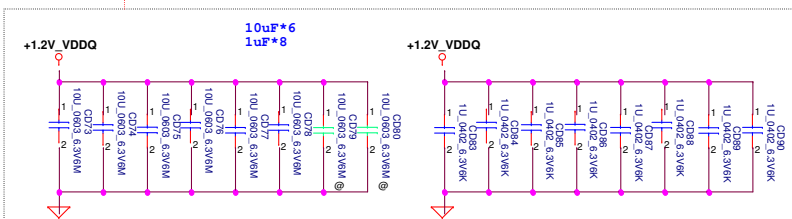
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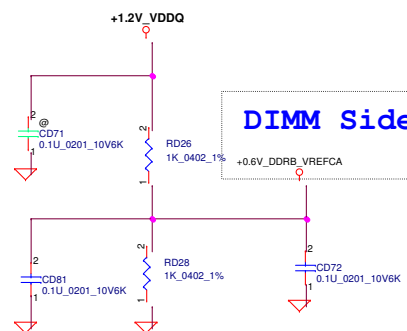
Layout Note:  
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2



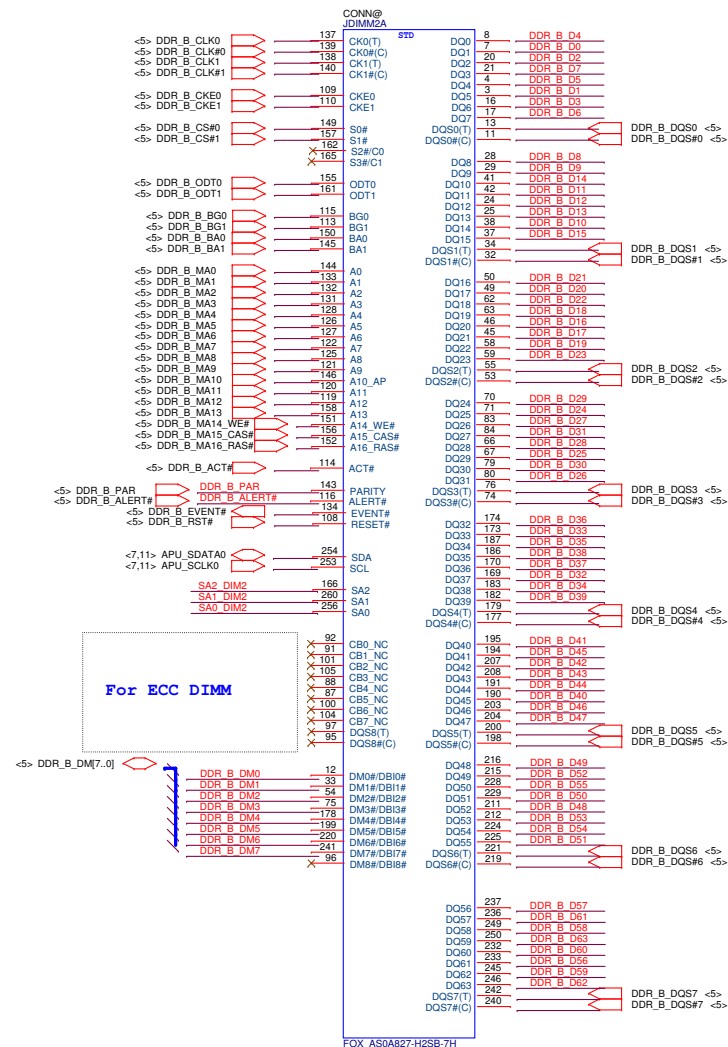
Layout Note:  
Place near JDIMM2



Part Number: LTCX0069FA0  
Part Value: S SOCKET FOX AS0A827-H2SB-7H 260P DDR4

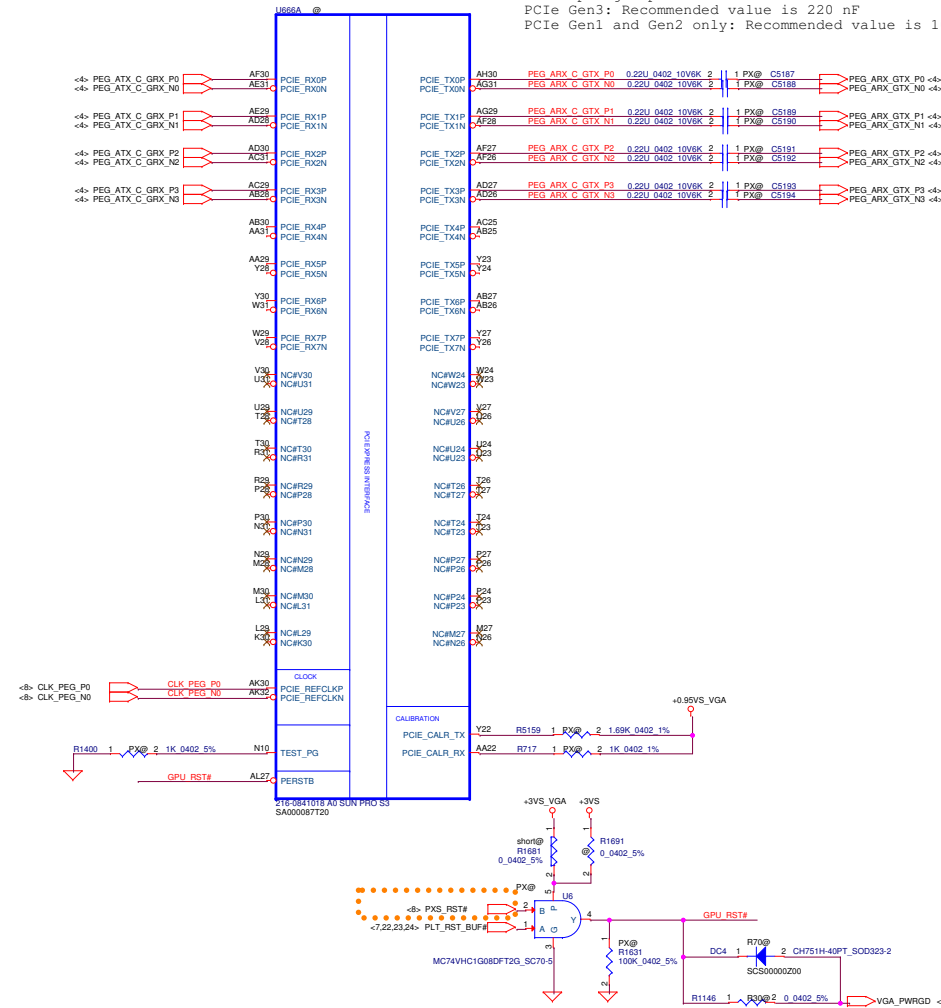


VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

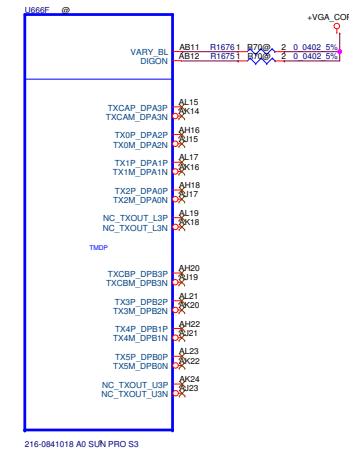


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P12-DDR4 CHA: JDIMM2				Rev
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AC Coupling Capacitor  
PCIe Gen3: Recommended value is 220 nF  
PCIe Gen1 and Gen2 only: Recommended value is 100 nF

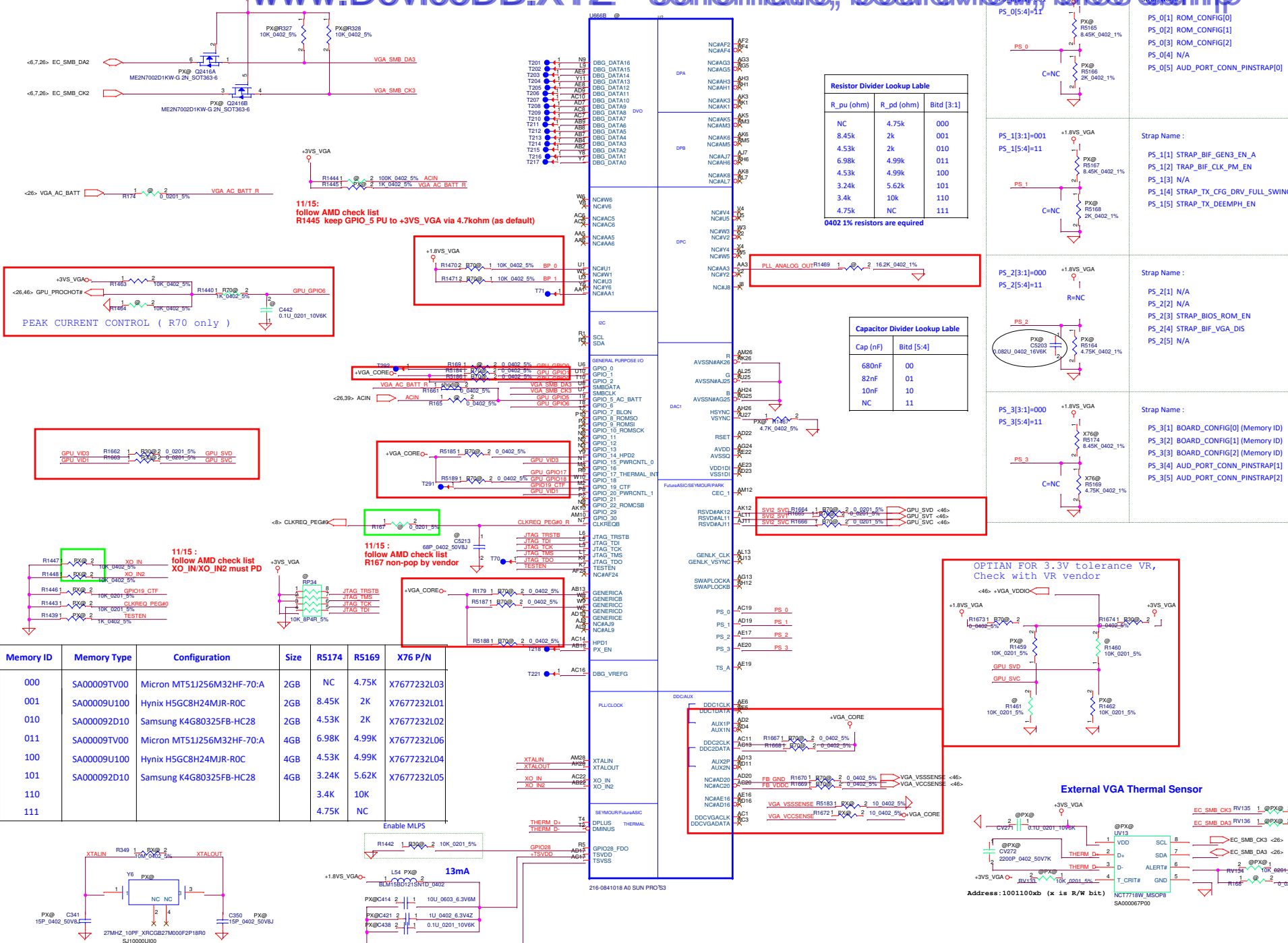


No Use GPU Display Port output

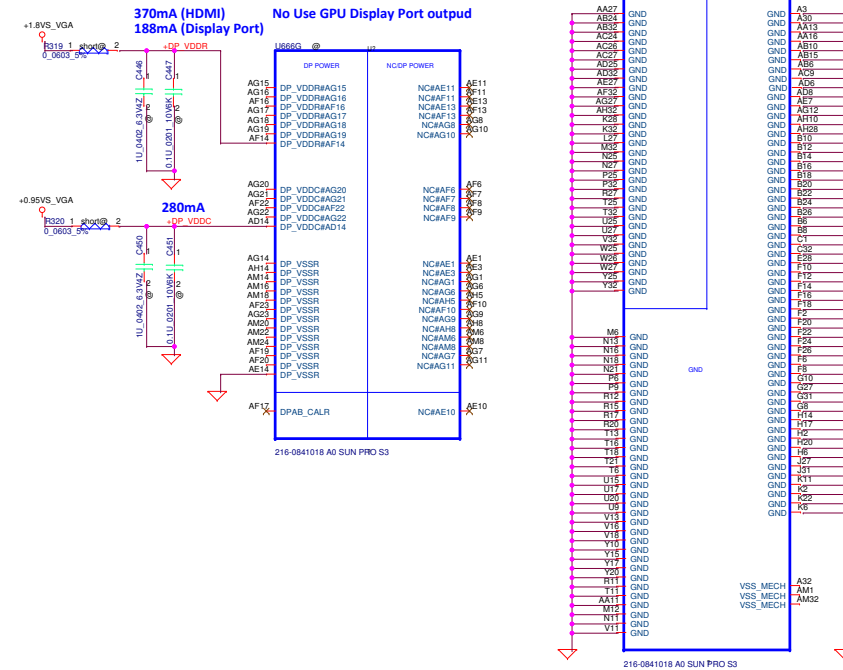


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				Customer	Weasley EPV21 LA-0376P	
				Material	Mater. No. 1000	
				Sheet	4 of 50	

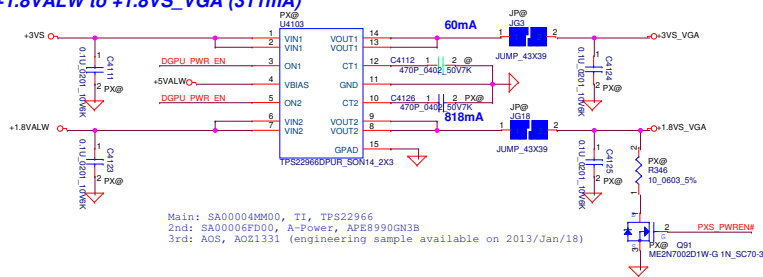




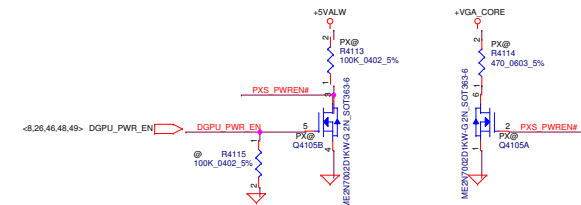
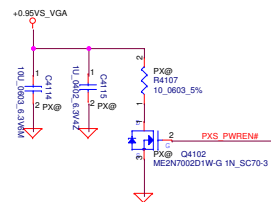
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				Month	Year	Sheet
				09	21	14 of 50



+3VS to +3VS\_VGA (25mA)  
+1.8VALW to +1.8VS\_VGA (311mA)

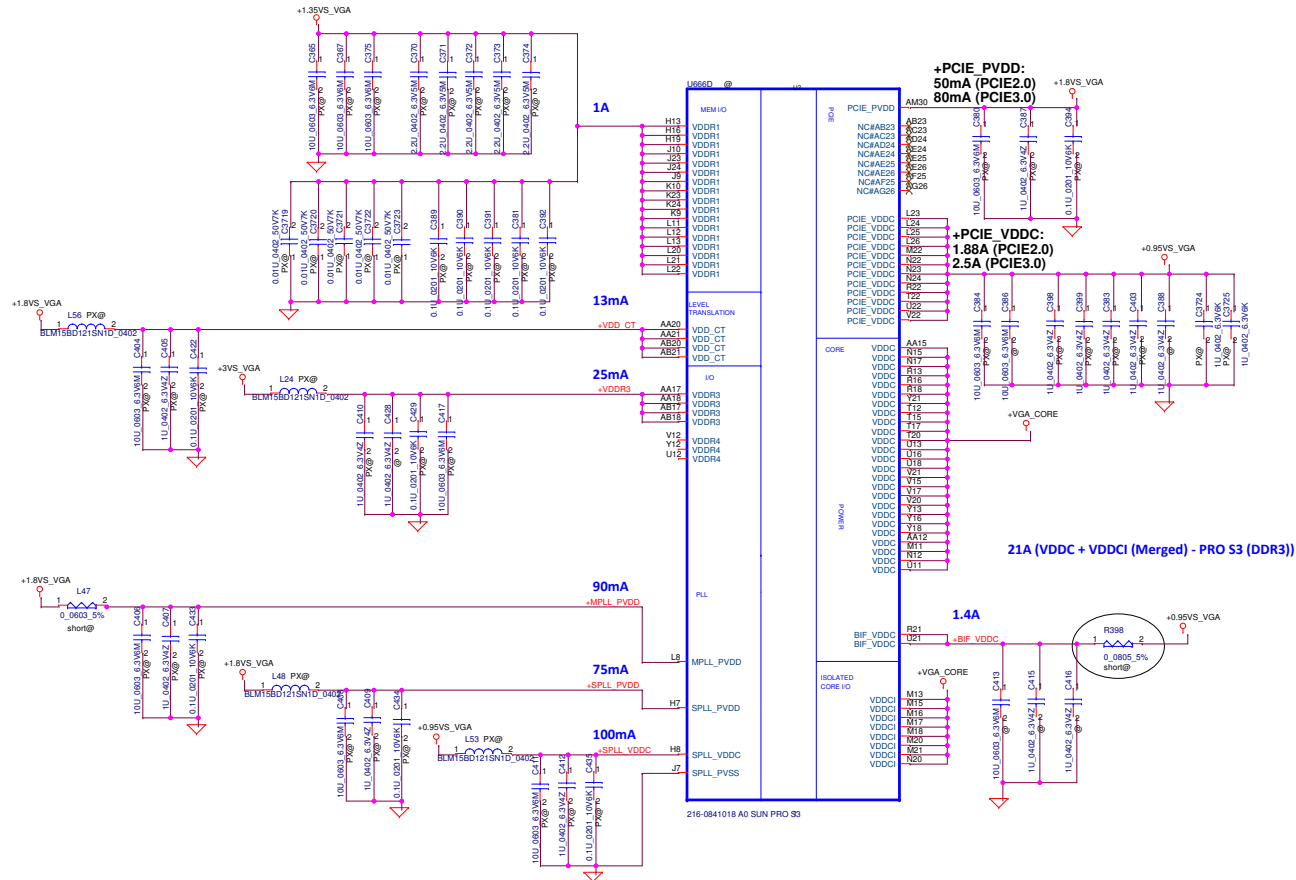


+0.95VSG (2A)



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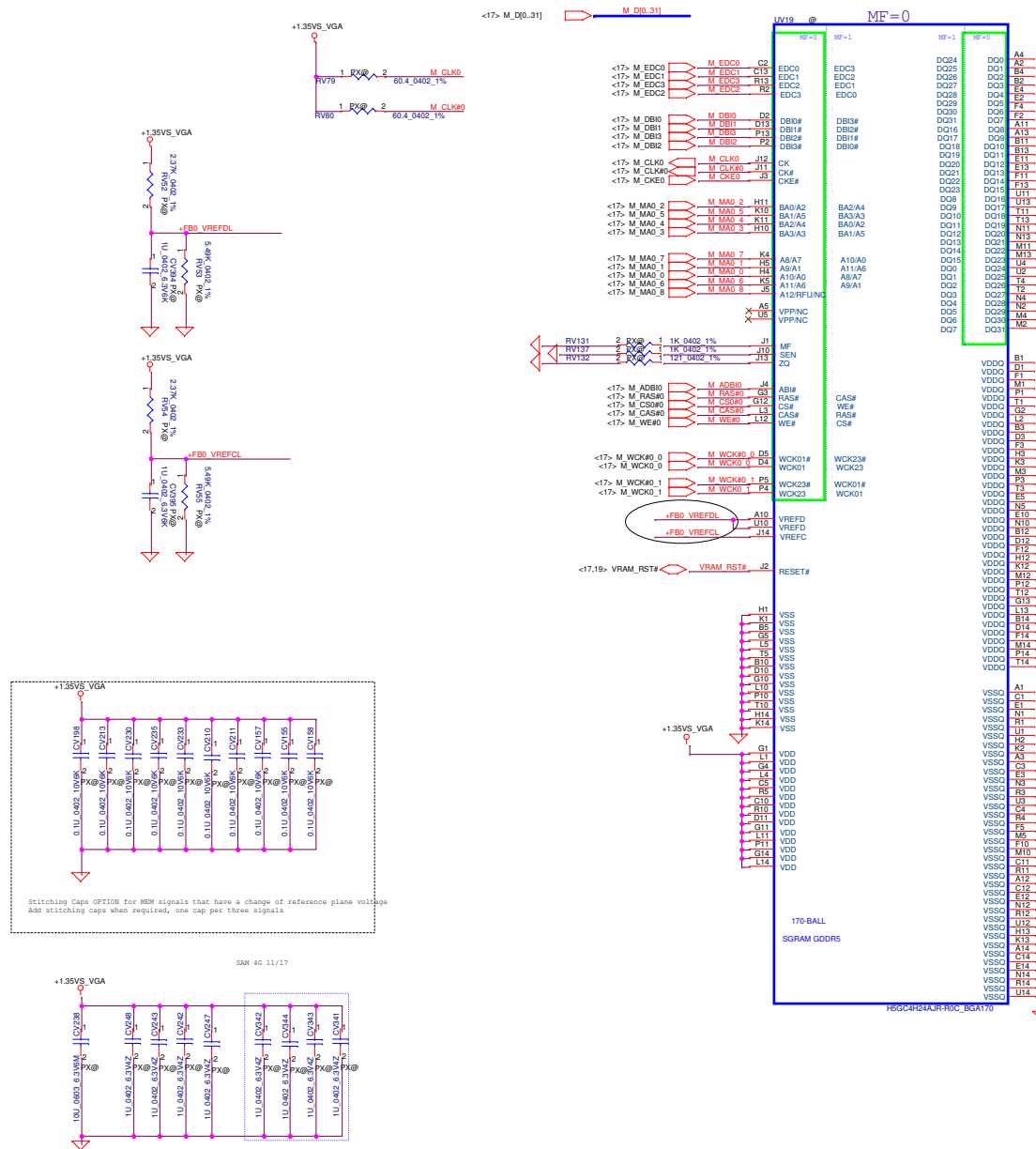
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VDDR3	25mA	0	2 (1@)	1



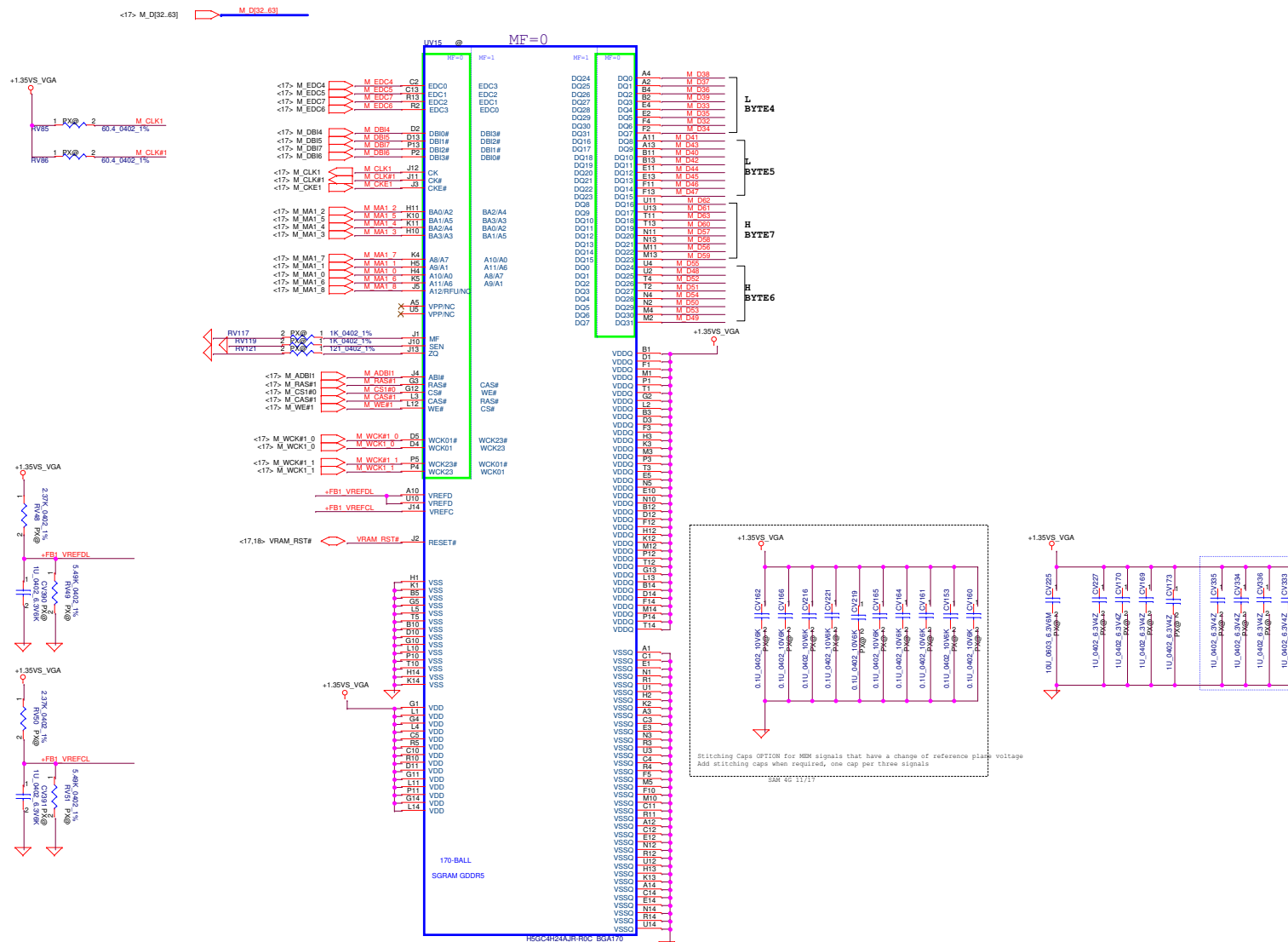
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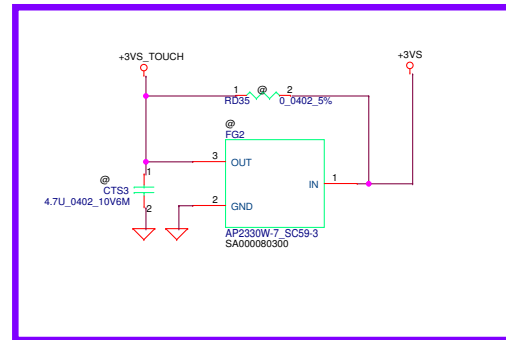
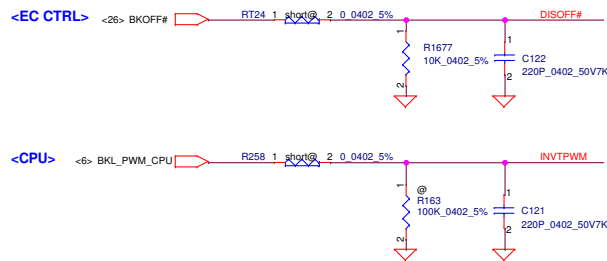
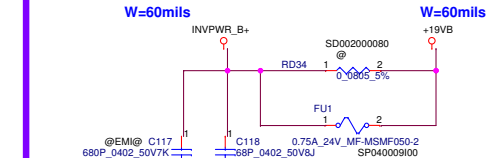
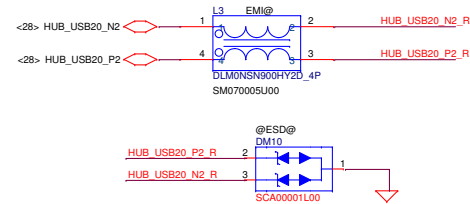




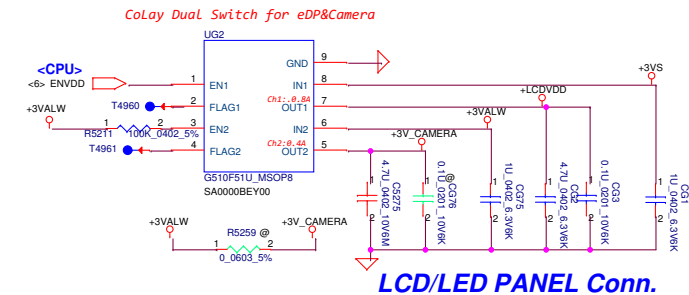
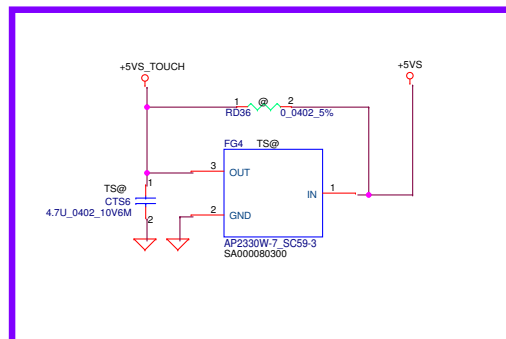
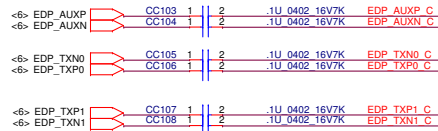


clamshell configuration 11/26



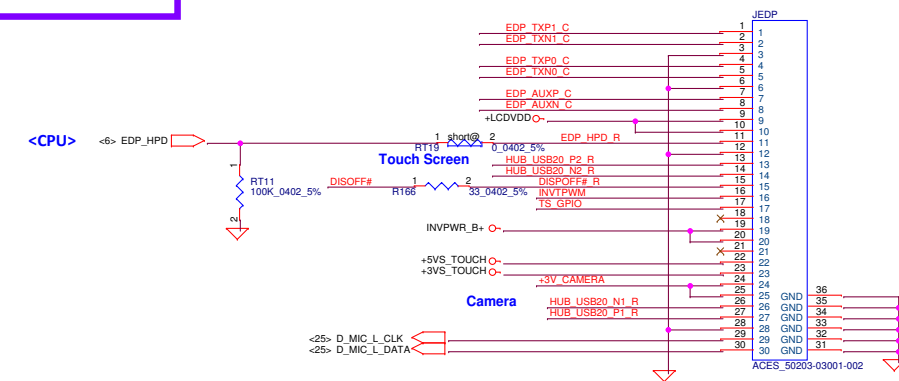
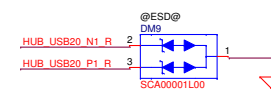
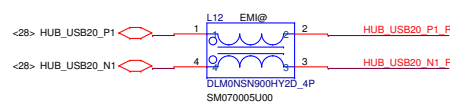


CC103~108 close JLVDS <1000mil

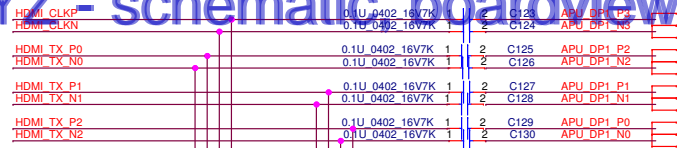
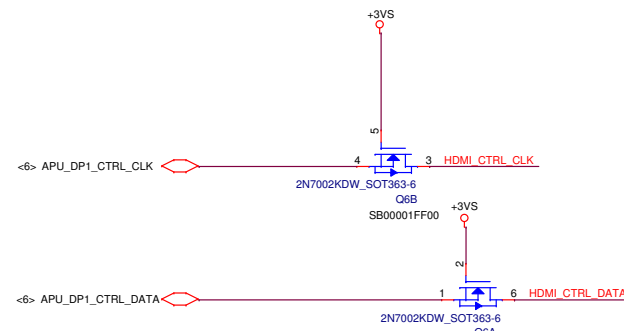


**LCD/LED PANEL Conn.**

## Camera



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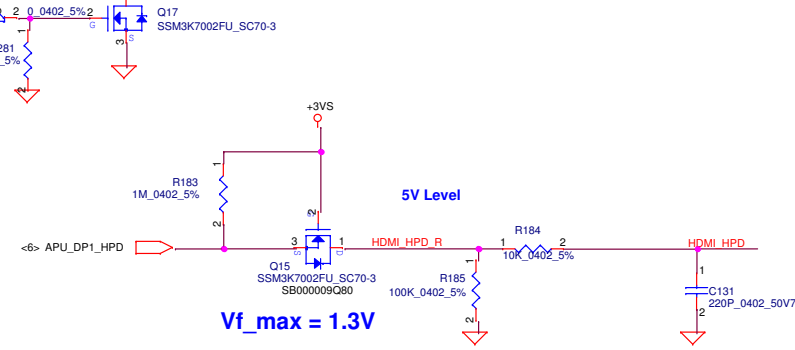
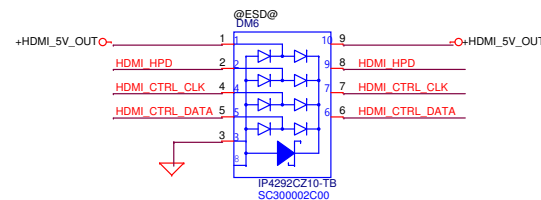
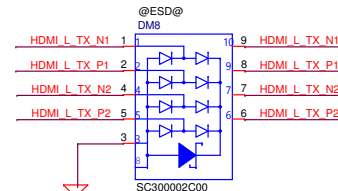
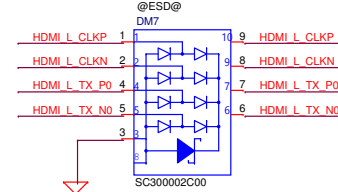
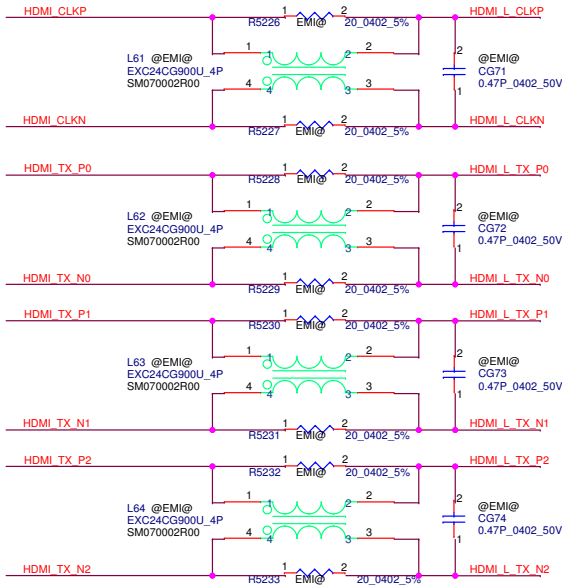
NET: HDMIRES\_GND  
WIDTH>20 mils

CLK

Data0

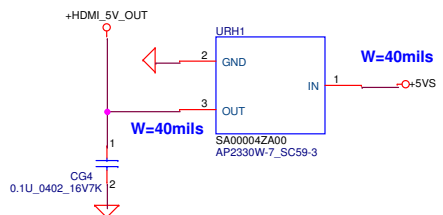
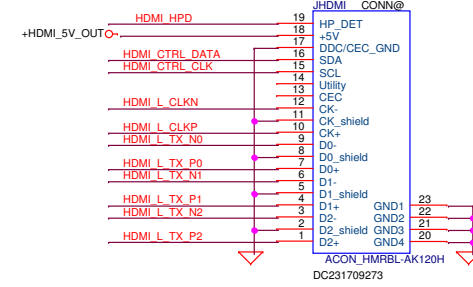
Data1

Data2



Vf\_max = 1.3V

HDMI Conn.

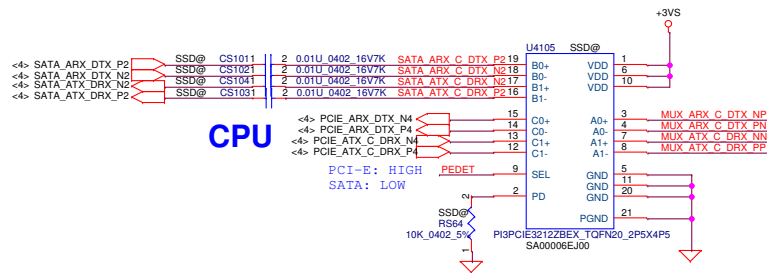


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# SSD

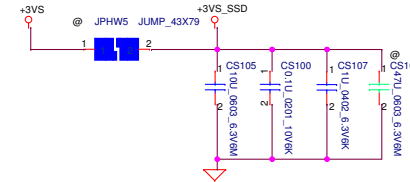
CPU



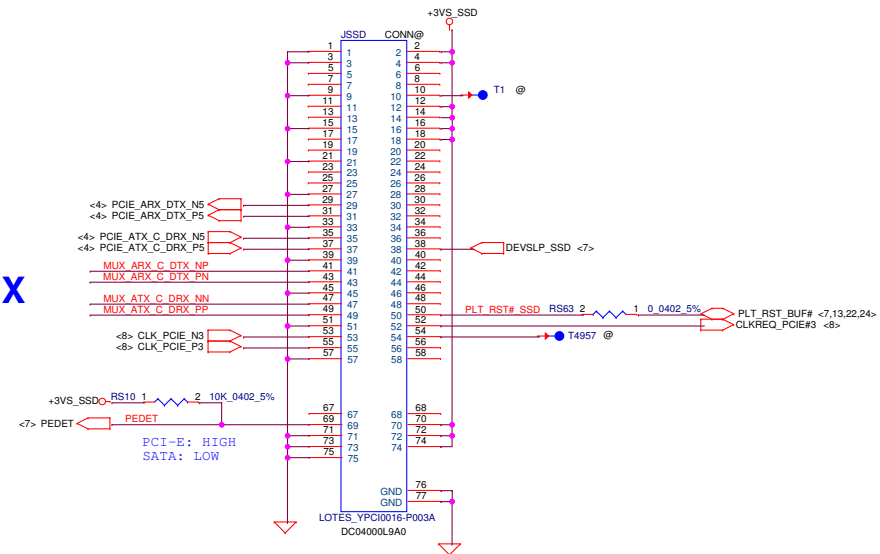
CPU

MUX

JPHW5 need to short

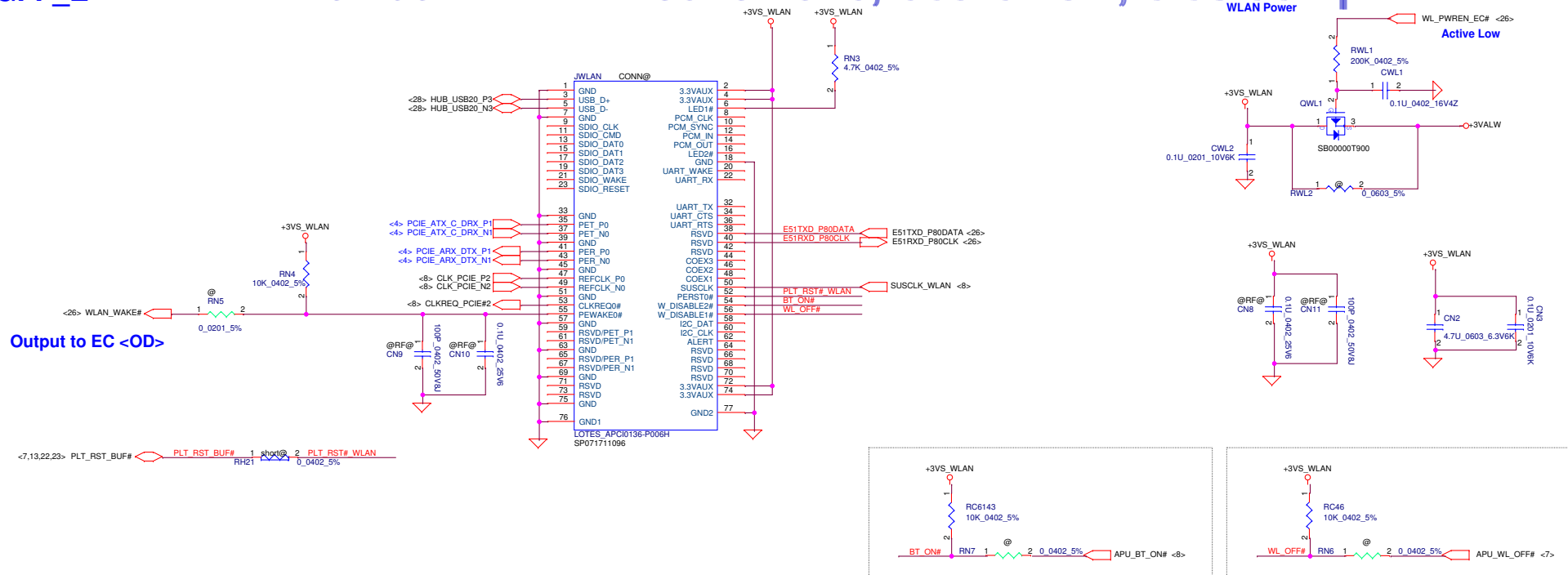


Key M



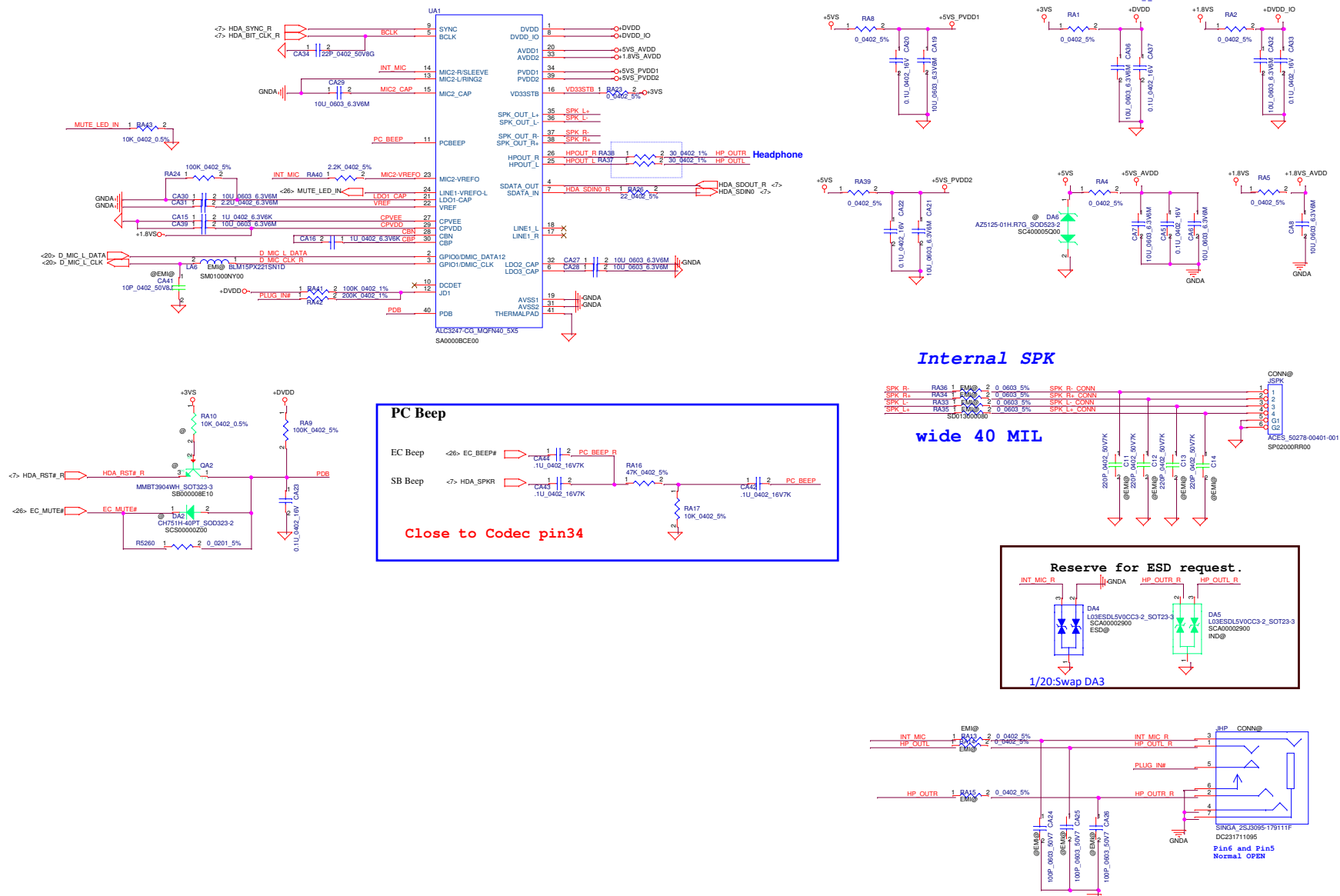
Truth Table

Function	SEL	PD
A to B	L	L
A to C	H	L
All ports Hi-Z, IC Power Down	X	H



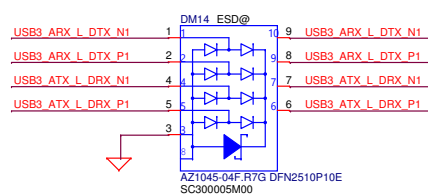
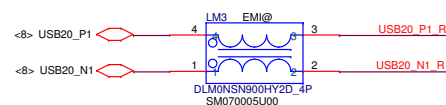
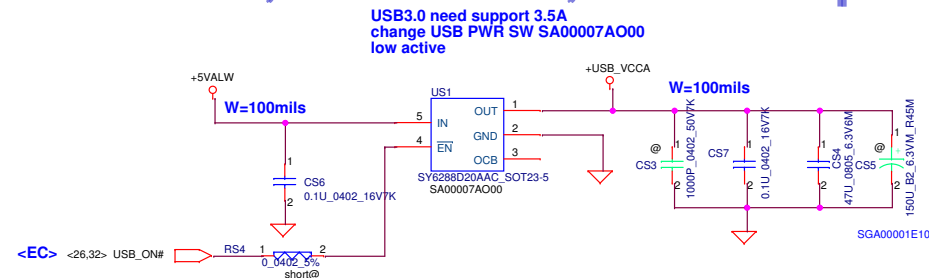
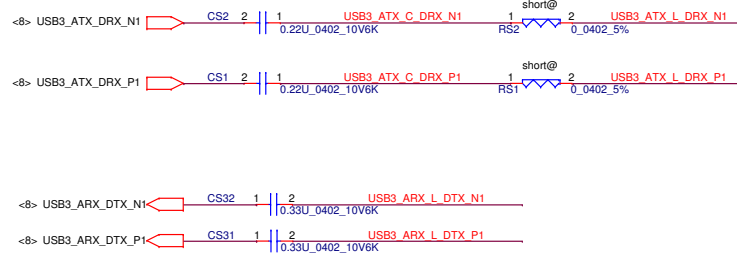
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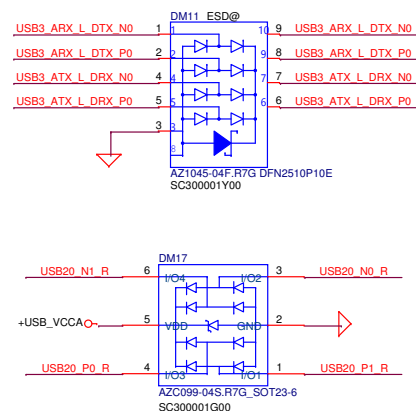
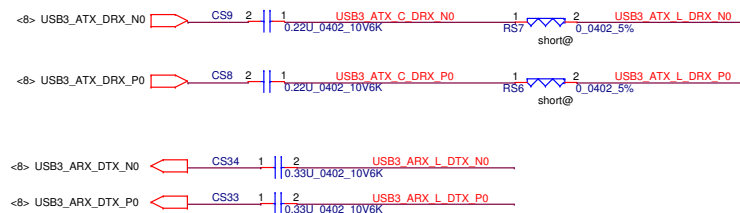
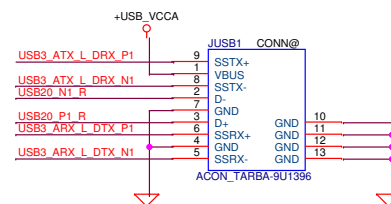




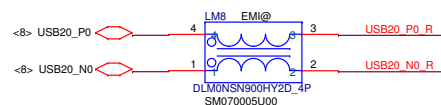
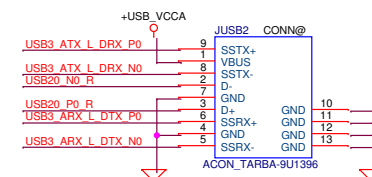
# USB3.0 port x 2



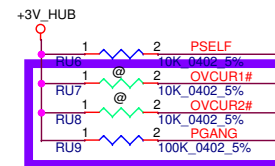
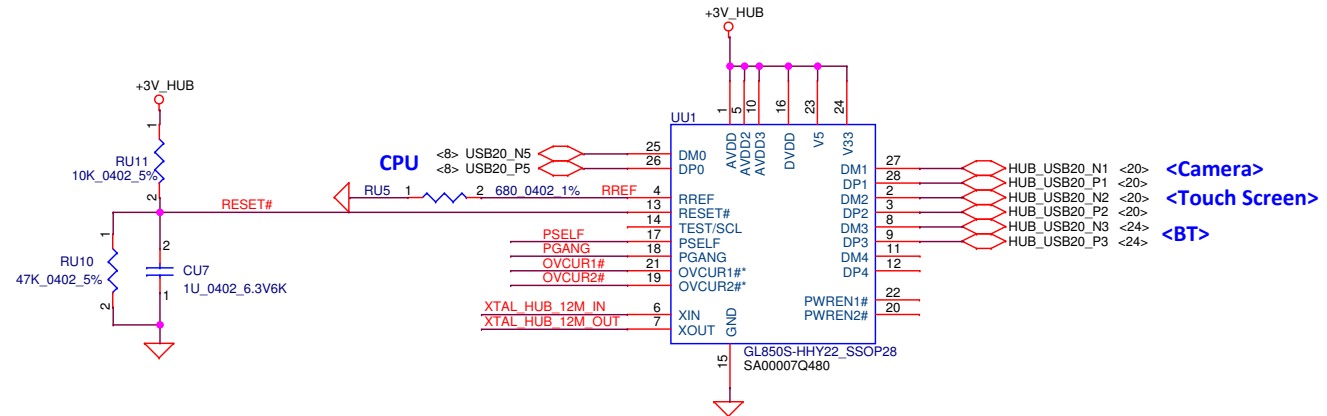
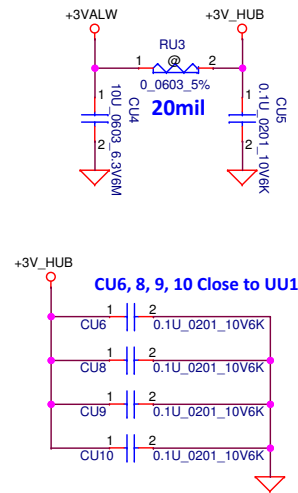
## USB2.0/USB3.0 port 1



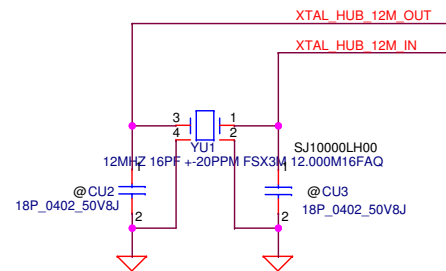
## USB2.0/USB3.0 port 0



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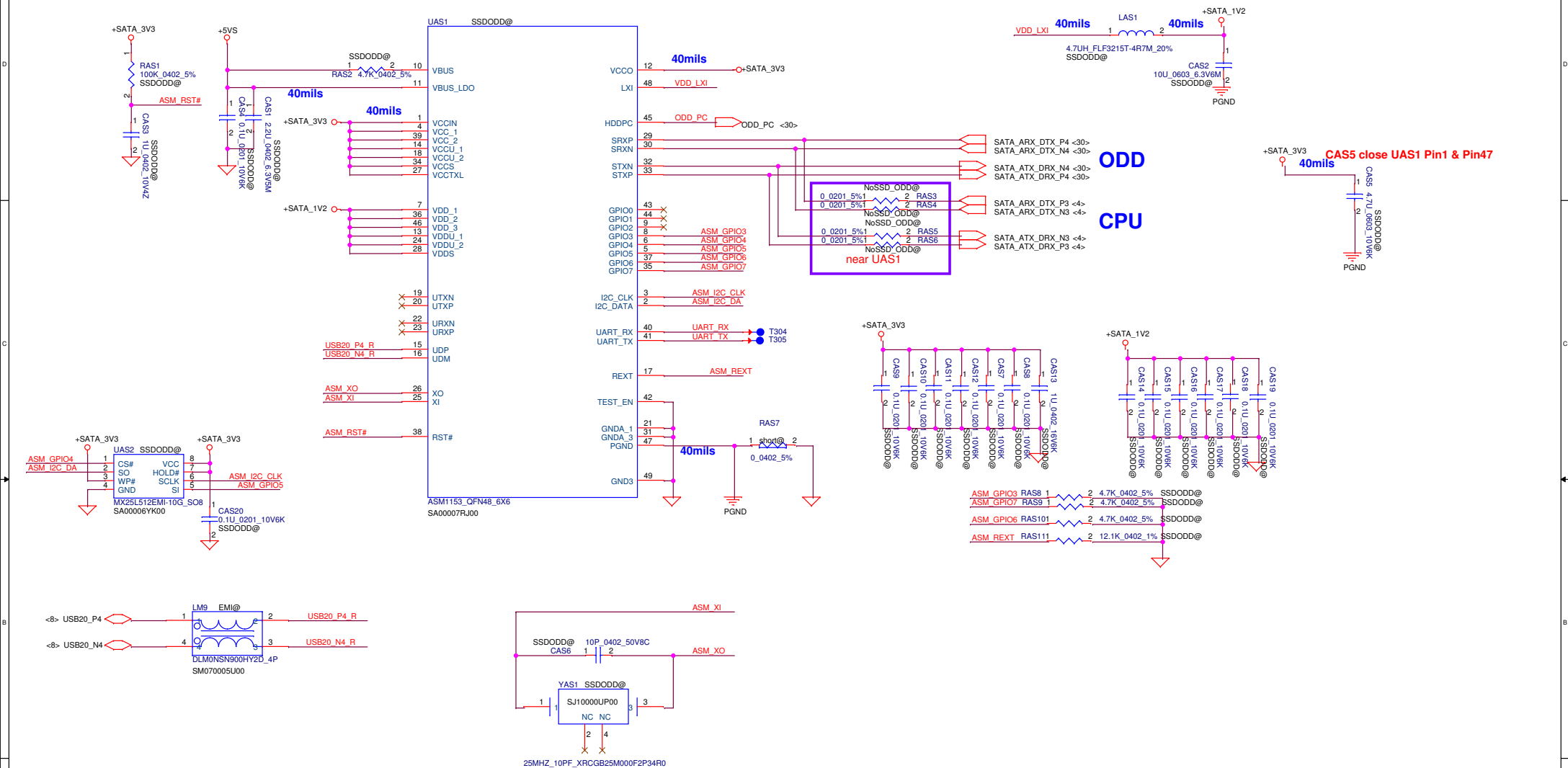


DB: change PGANG to PU for Gang mode  
Unpop RU6&7 for unuse OCP

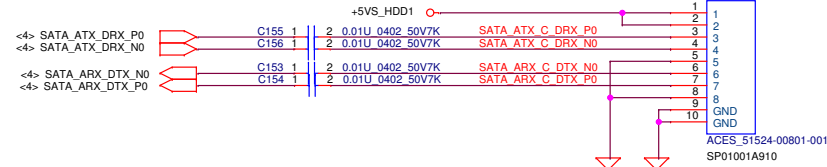
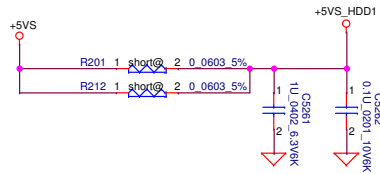


Vender review:CU2, CU3 cap no install

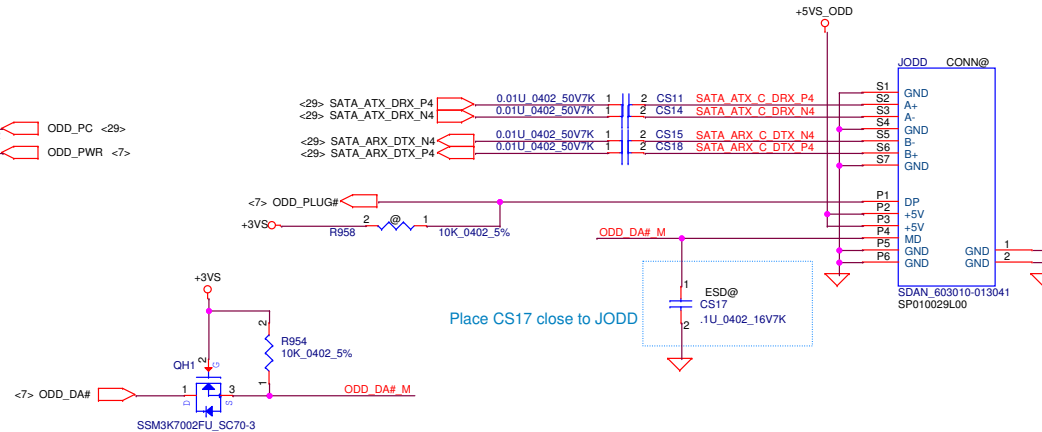
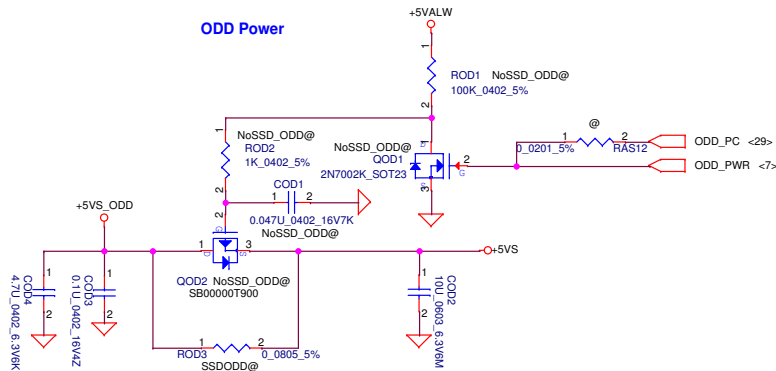
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## 2.5" SATA HDD connector

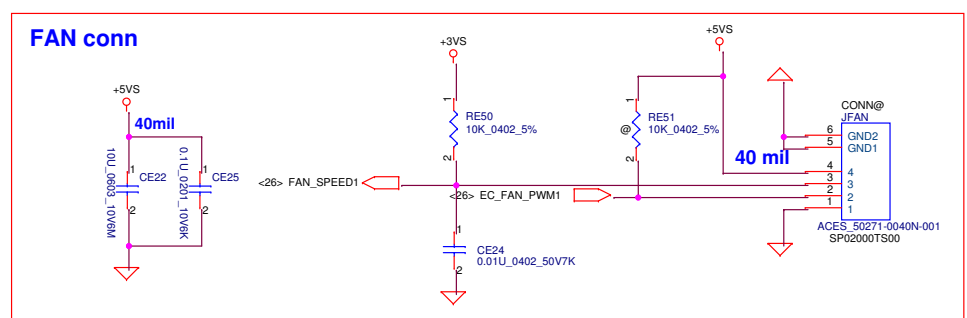
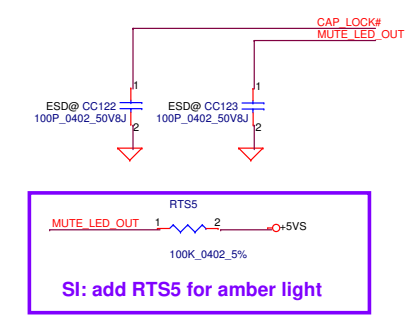
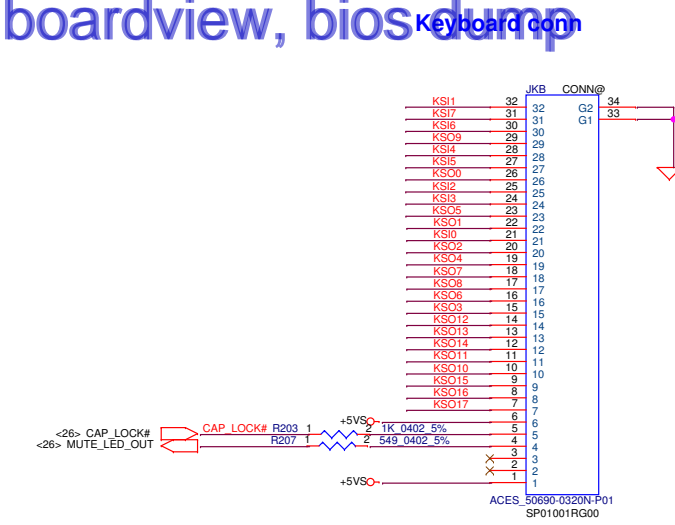
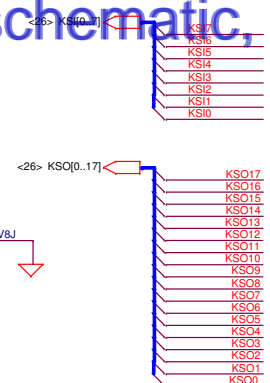
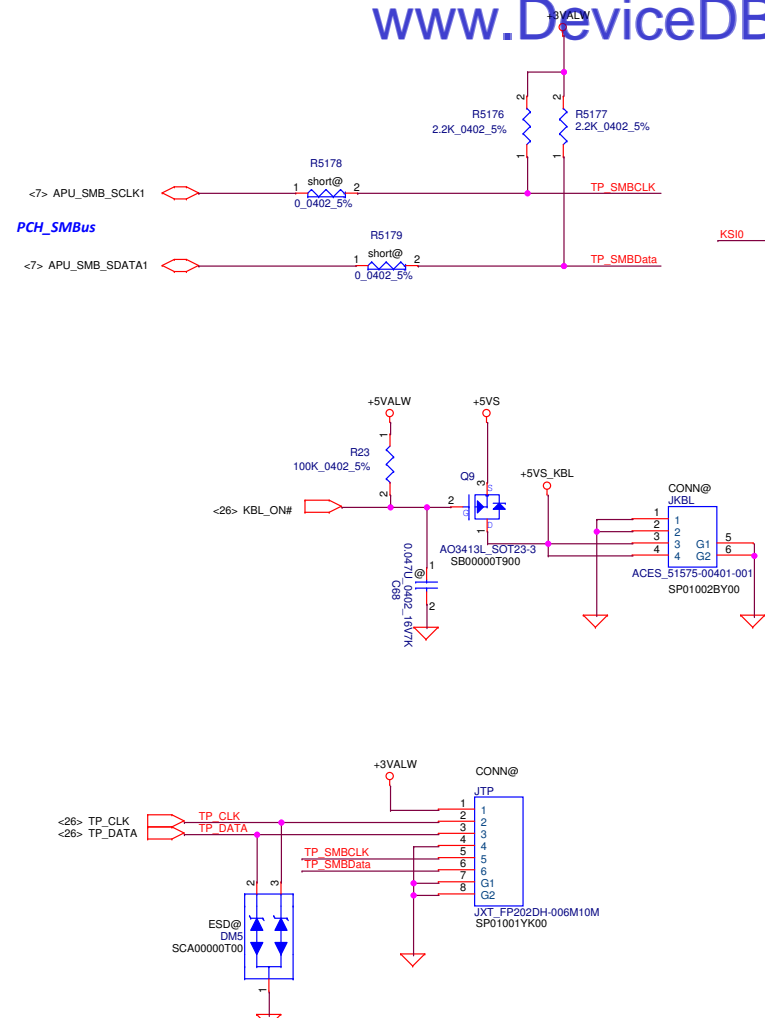


## ODD Power

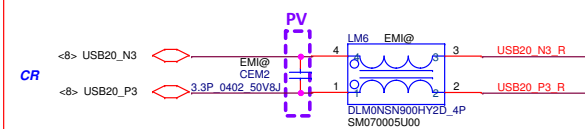


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PCH\_SMBus



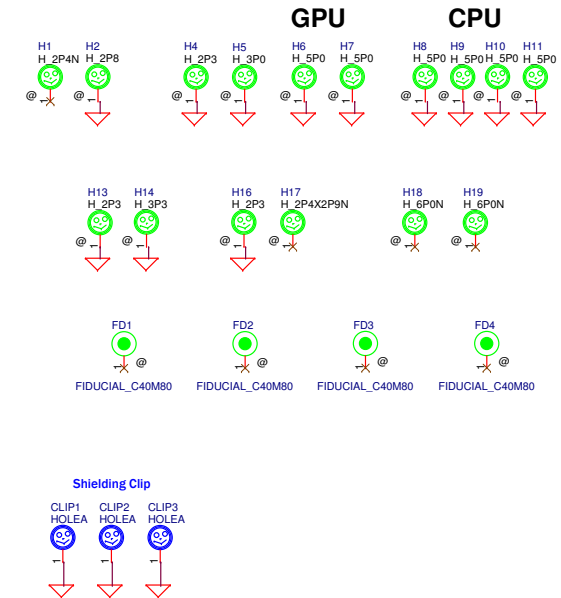
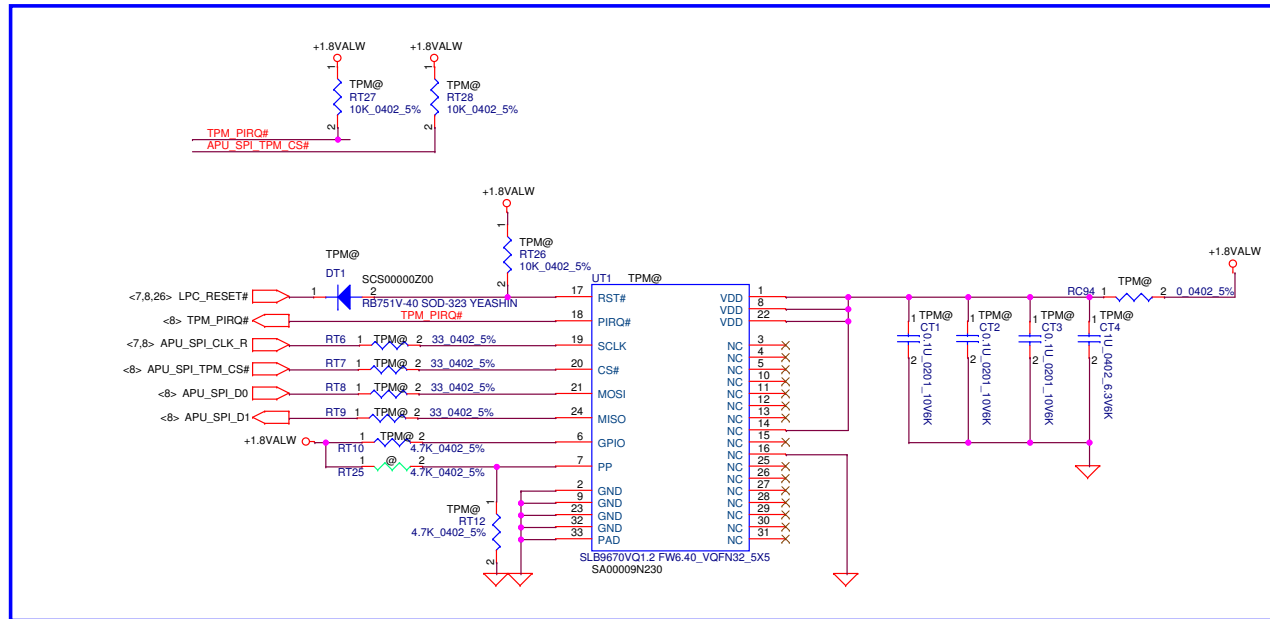
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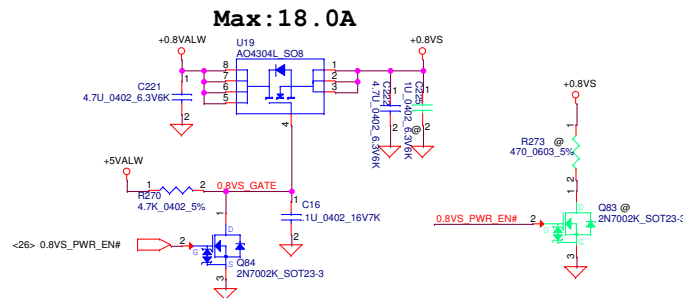
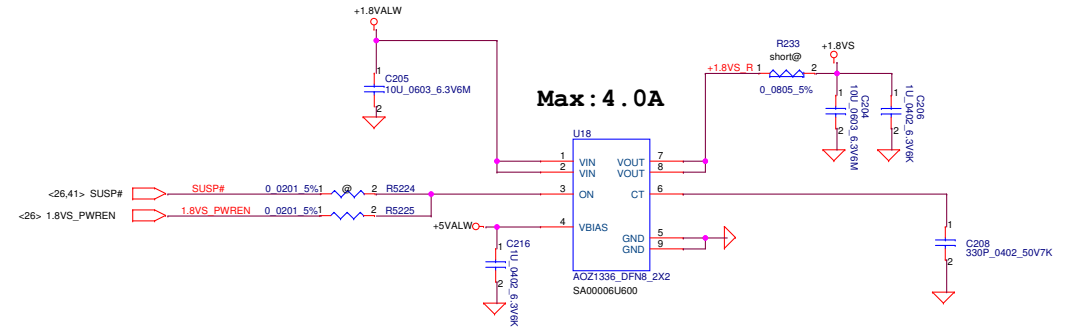
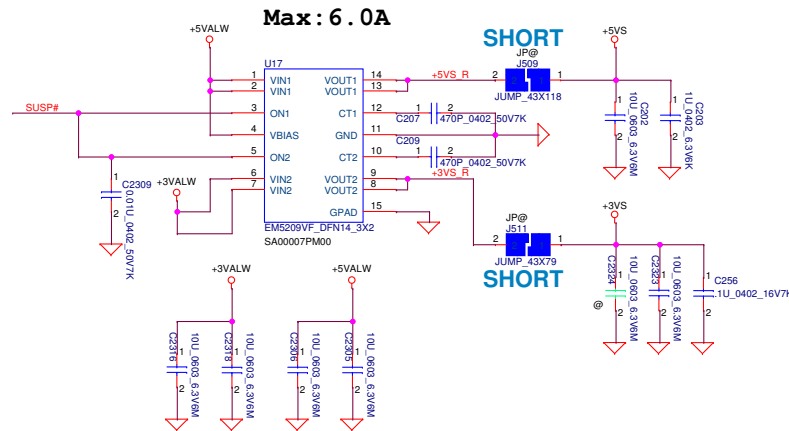
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# TPM2.0

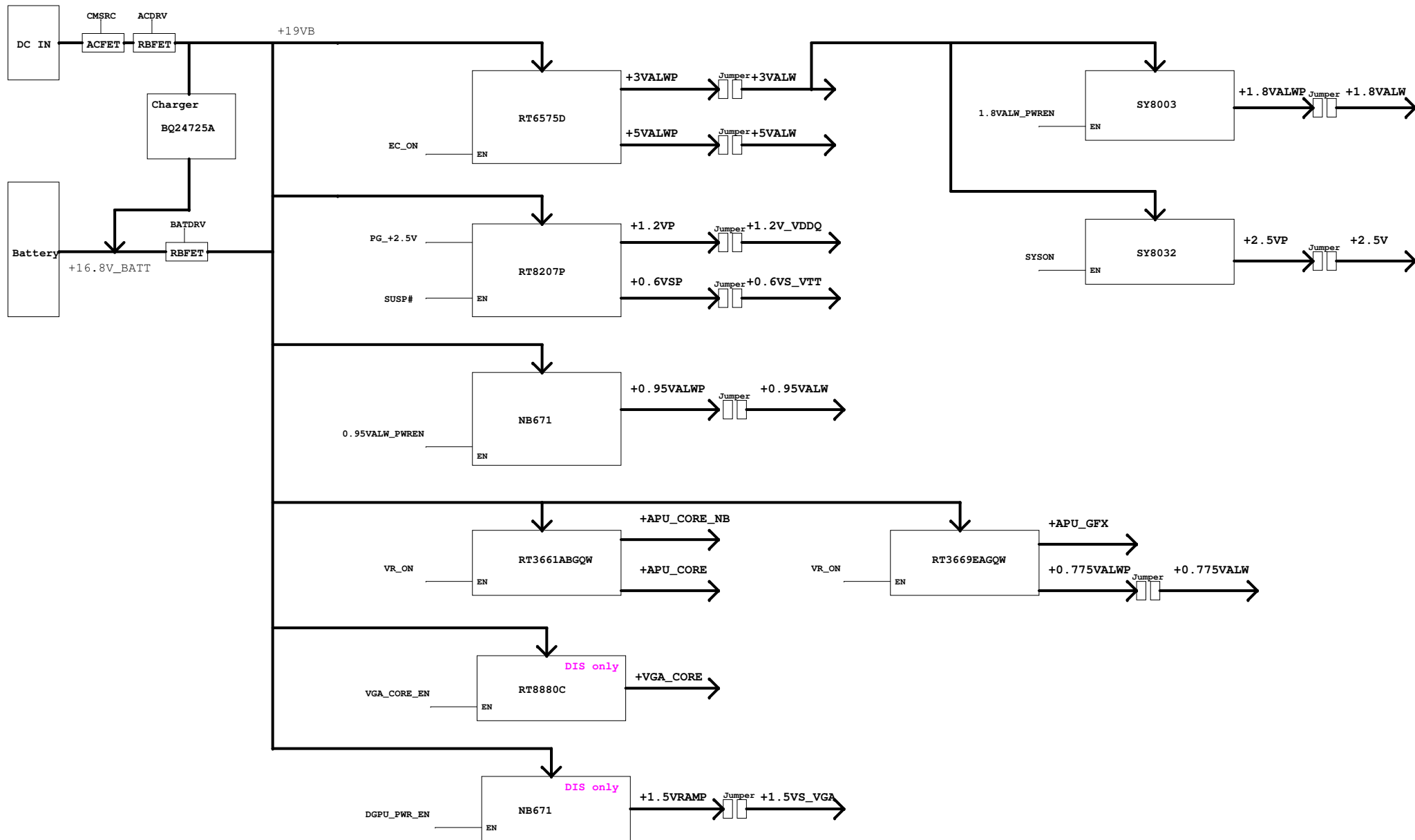


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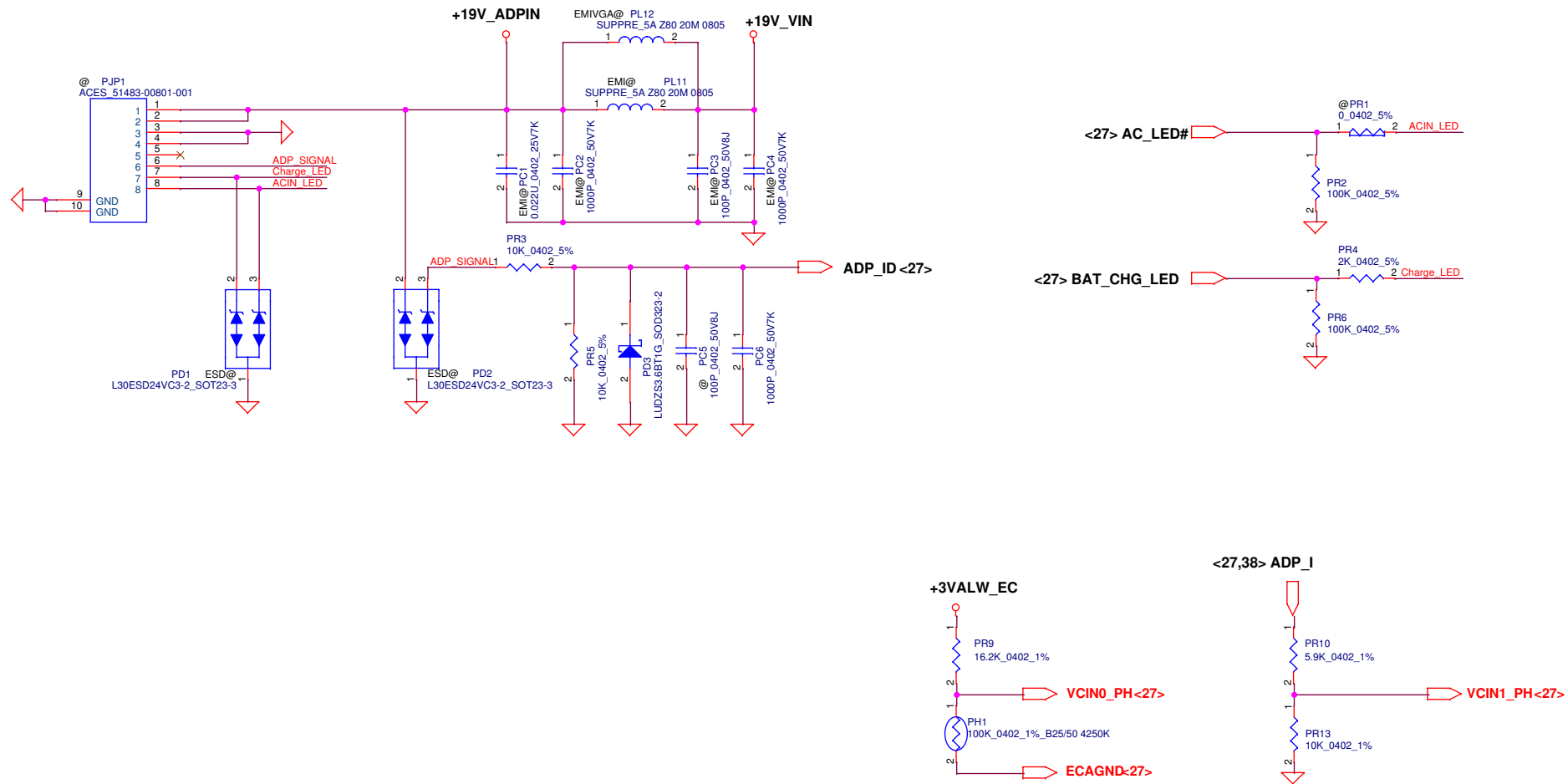


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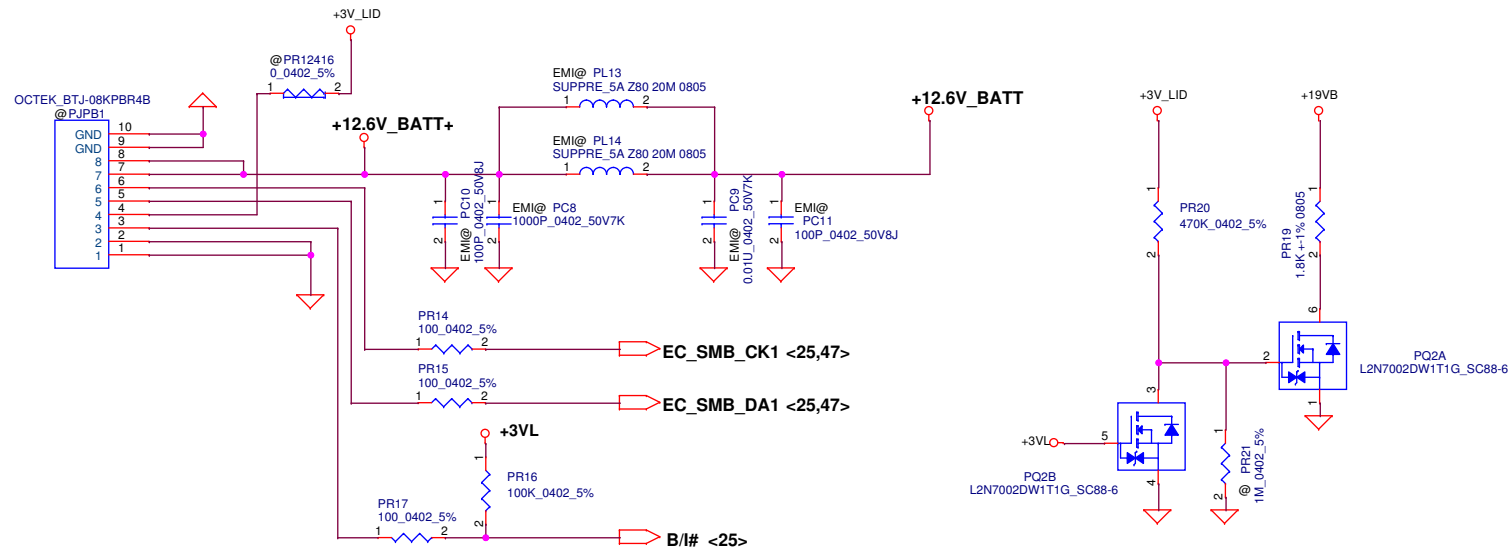




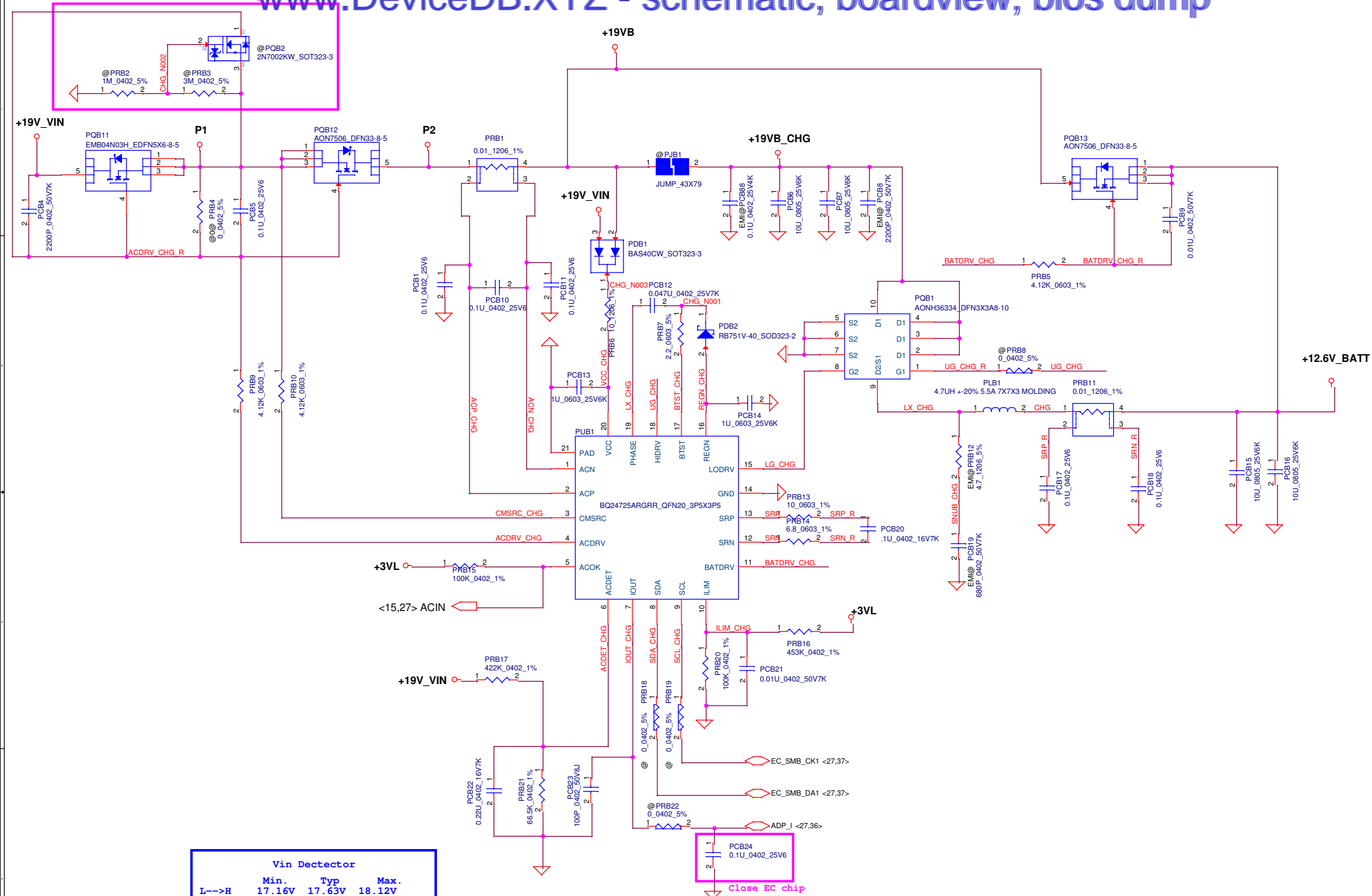
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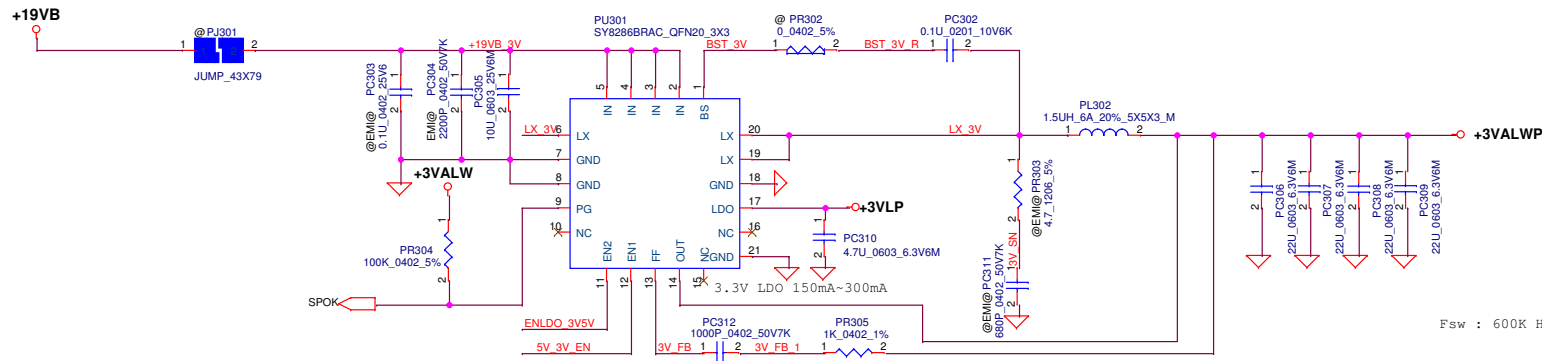


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				Rev	0.1



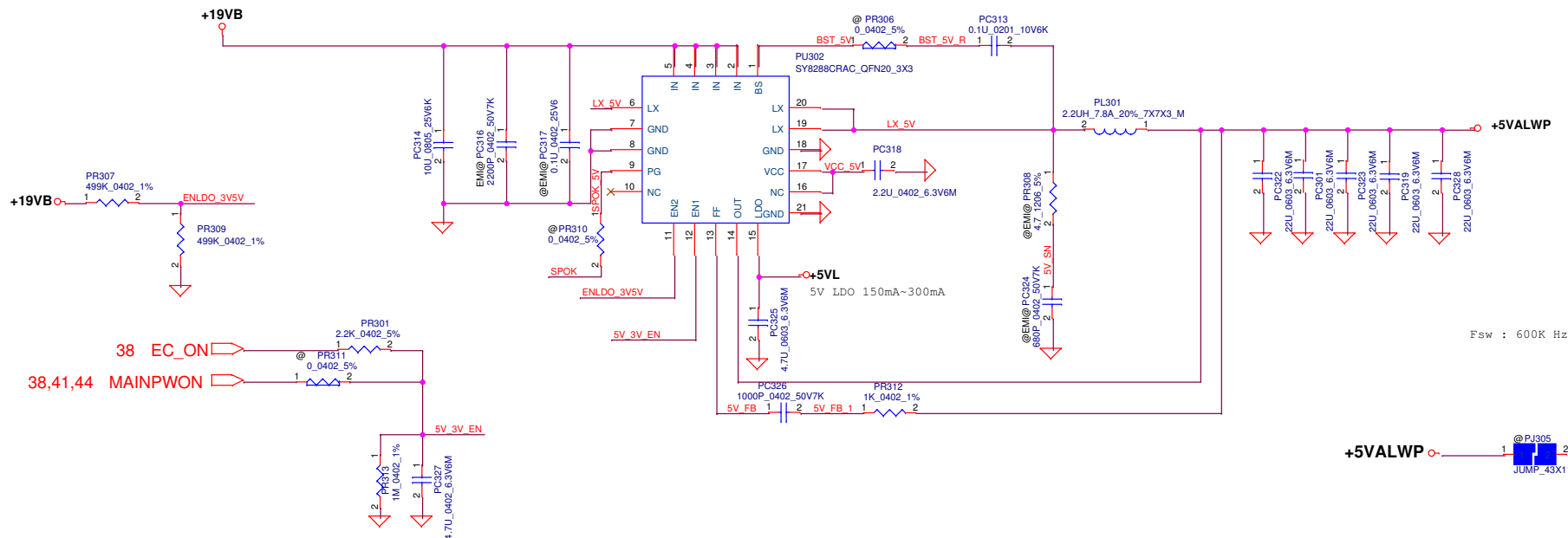
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+3VALWP → JUMP\_43X118 → +3VALW

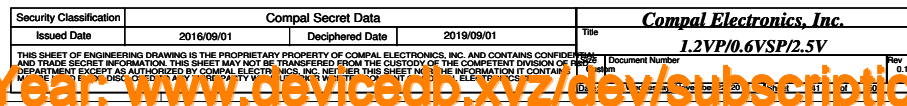
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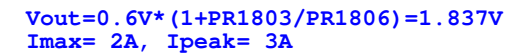


+5VALWP → JUMP\_43X118 → +5VALW

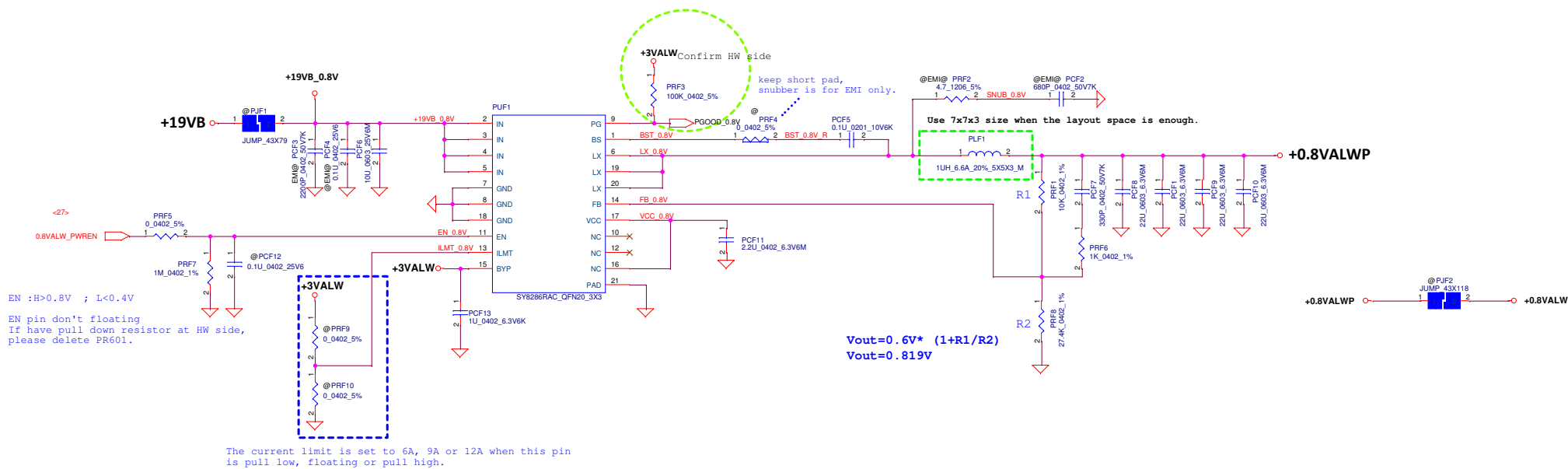
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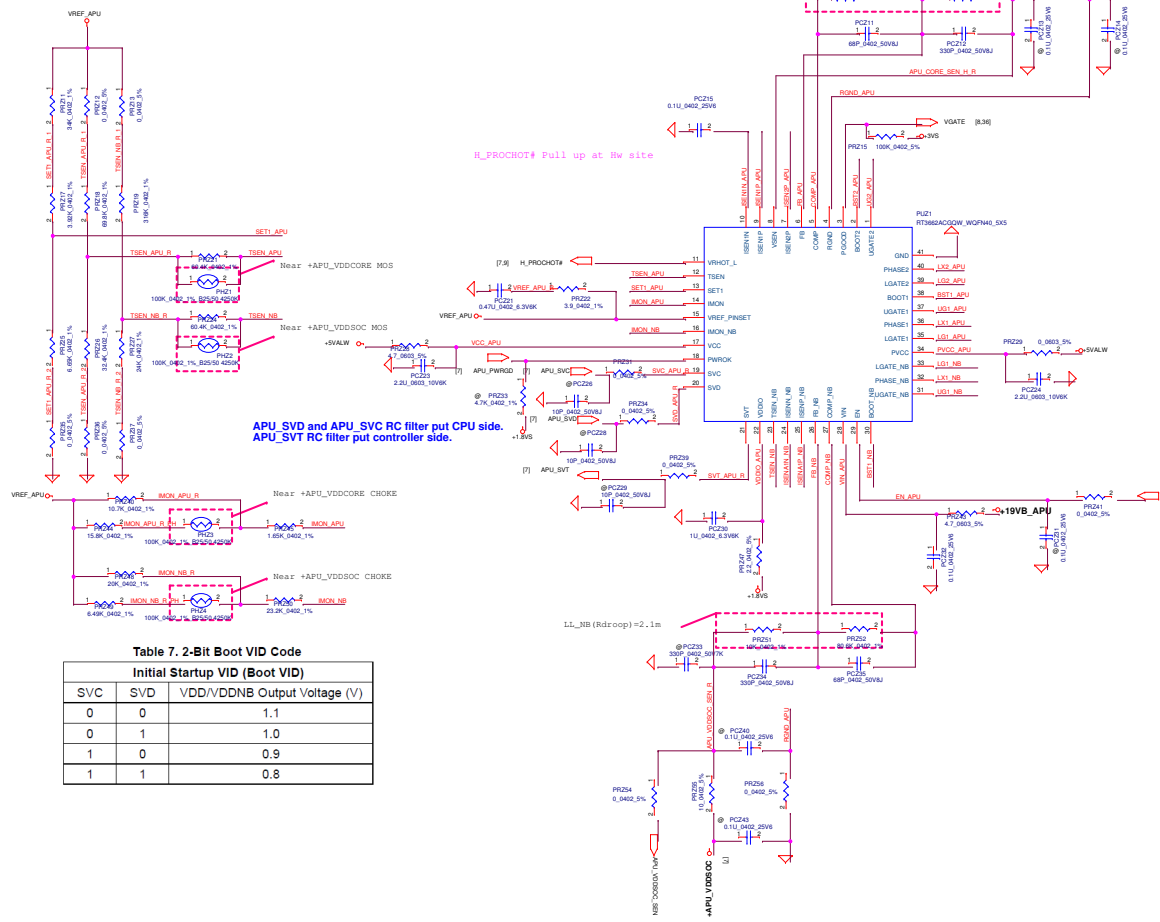
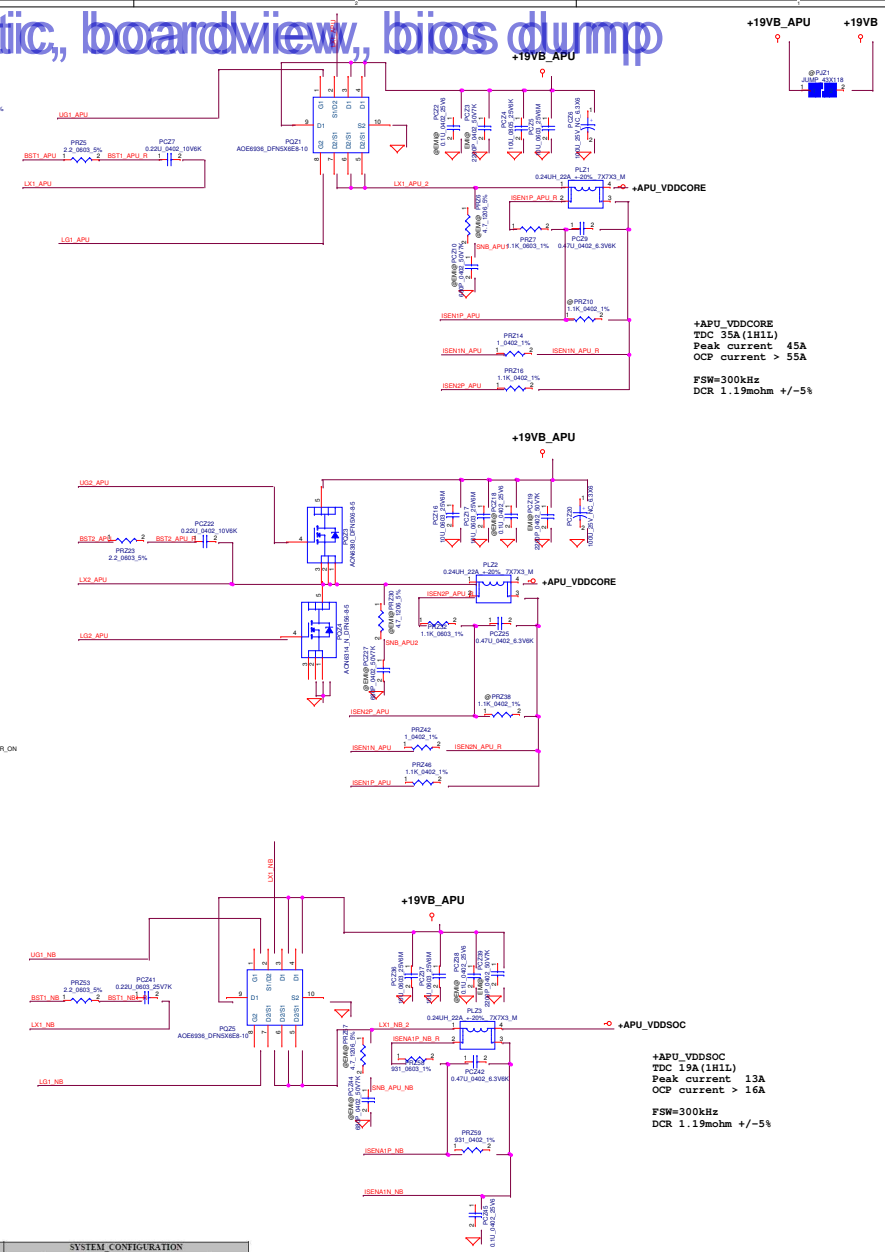


Table 7. 2-Bit Boot VID Code

Initial Startup VID (Boot VID)		
SVC	SVD	VDD/VDDNB Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Table 5. FP5 Processor Voltage Supply Current

		Nominal Voltage at Pkg Ball (V) <sup>2</sup>	Condition	SYSTEM CONFIGURATION					
Supply <sup>1</sup>				1 12W	2 15W	3 25W	4 35W	5 45W	6 54W
Variable (0.65~TBD) <sup>3</sup>		EDC	38	45	70	85	85	64	
VDDCR_VDD	Max Loadstep <sup>4</sup>	TDC <sup>3</sup>	35	35	56	56	68		
					10				
Variable (0.72~TBD) <sup>3</sup>		EDC			13				
VDDCR_SOC	Max Loadstep <sup>4</sup>	TDC <sup>3</sup>			10				



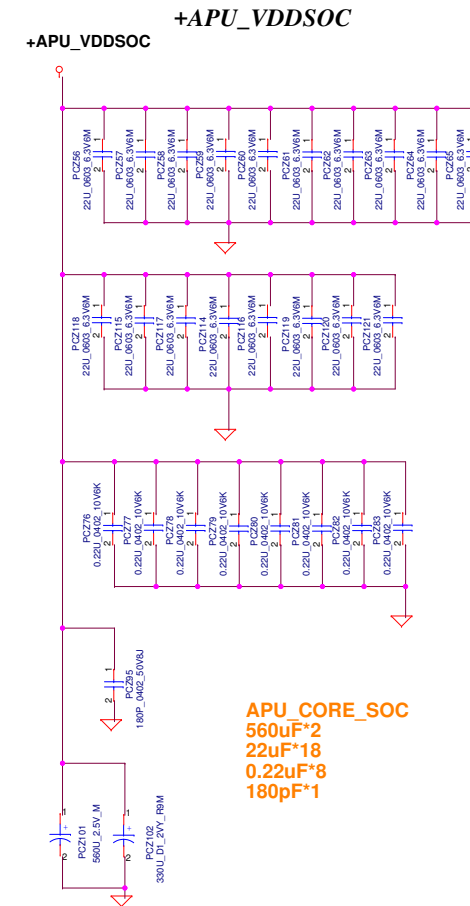
```
+APU_VDDCORE
TDC 35A(1H1L)
Peak current 45A
OCP current > 55A

FSW=300kHz
DCR 1.19mohm +/-5%
```

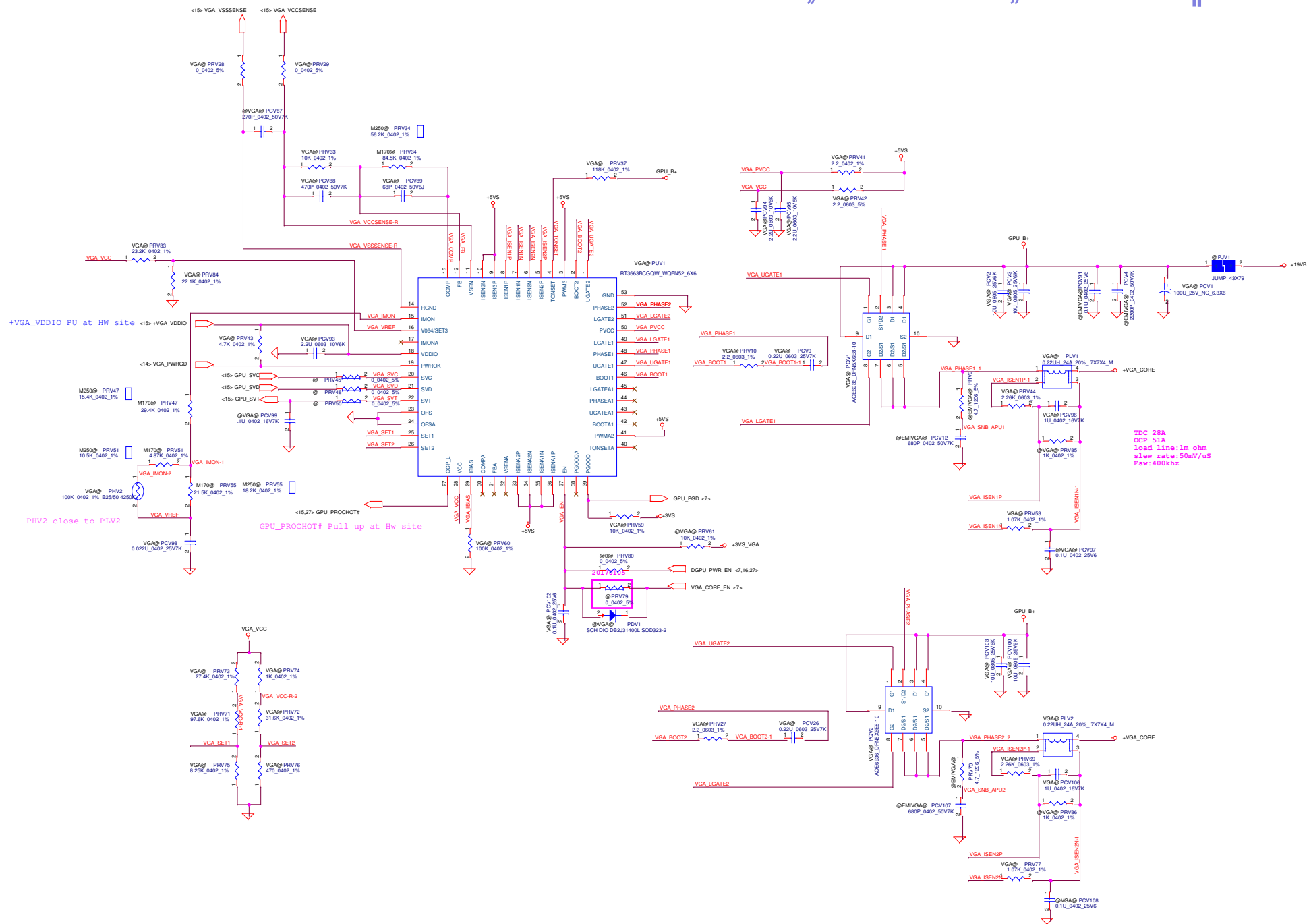
```
+APU_VDDSOC
TDC 19A(1H1L)
Peak current 13A
OCP current > 16A

FSW=300kHz
DCR 1.19mohm +/-5%
```

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			PWR_APU_CORE/APU_CORE_NB	

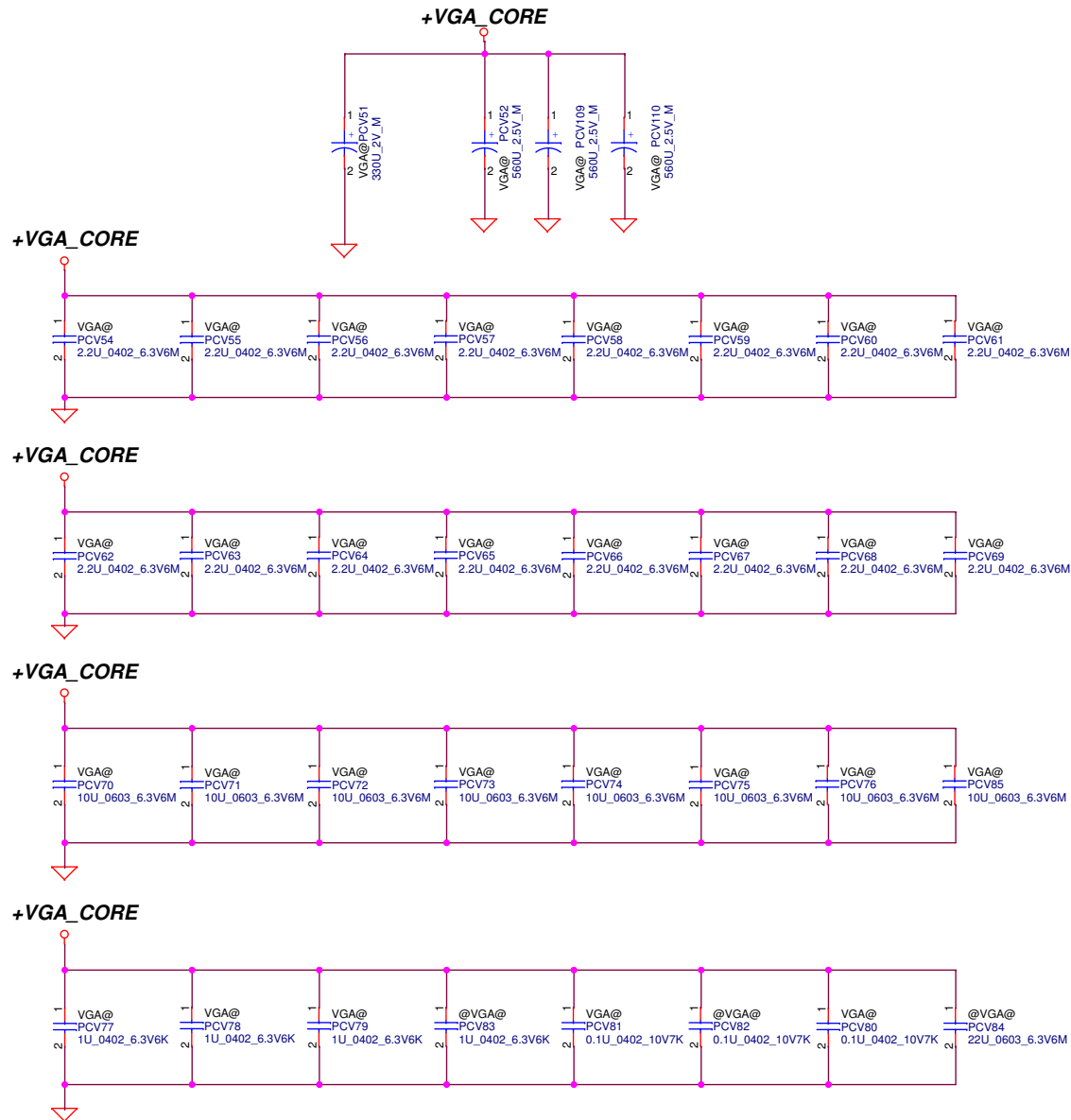


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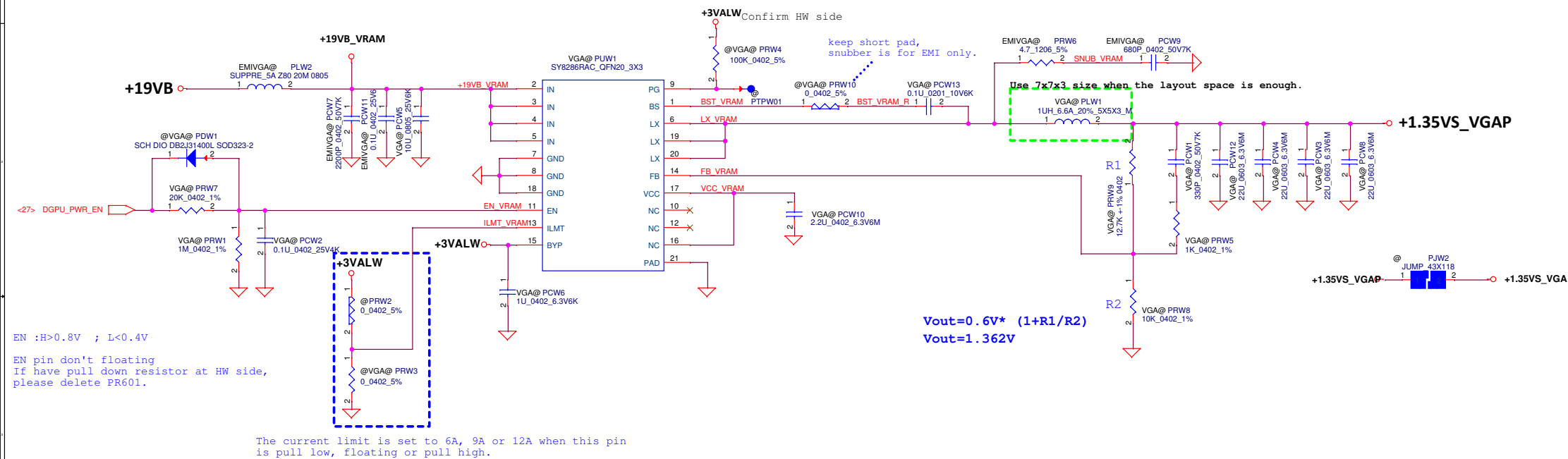
TDC 28A  
OCP 51A  
load line: 1m ohm  
slew rate: 50mV/us  
Fw: 400kHz

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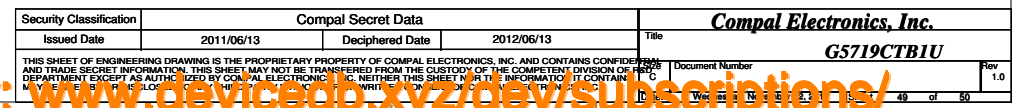


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Version change list (P.I.R. Lists)

SI  
6L M170 X63AB982L01 X4PAB982L01  
8L M170 X63ABI32L01 X4PABI32L01

Itm	Page	Title	Change Description	Date
1	39,41	Change to Main source	Change P051, P061 from EMI00000000 to A000000000	2017/11/10
2	44	Change to common use part	Change PC25, PC25, PC242 from 0.47U 25V 0402 size (SE000000000) to 0.47U 6.3V 0402 size (SE124474030)	2017/11/10
3	32	Change to Main source	Change P051 from A000000000 to EMI000000000	2017/11/10
4	43,44	Change to 0603 size (Layout space)	Change PC95, PC117, PC235 PC237 from 10uF 0805 size (SE000000000) to 10uF 0603 size (SE000000000)	2017/11/13
5	40,44	Change to 0603 size (Layout space)	Change PC305, PC25, PC216 from 10uF 0805 size (SE000000000) to 10uF 0603 size (SE000000000)	2017/11/13
6	44	Change to 0603 size (Layout space)	Change PC27, PC222 from 0.22uF 0402 size (SE03324280) to 0.22uF 0402 size (SE005224000)	2017/11/13
7	46	Change VDA solution (Vendor not support)	M170: Change P071 from RT8880C (SA000000000) to RT3063BC (SA000000000) FR053 from unpop to pop 23.2K 0402 size (SD034232280) FR054 from unpop to pop 22.1K 0402 size (SD034232280) Change PC008 from 0.47uF 0402 size (SE124474030) to 0.022uF 0402 size (SE075223030) Change FR054 from 100K 0402 size (SD034100080) to 84.5K 0402 size (SD034045030)  M250: Change P071 from RT8880C (SA000000000) to RT3063BC (SA000000000) FR053 from unpop to pop 23.2K 0402 size (SD034232280) FR054 from unpop to pop 22.1K 0402 size (SD034232280) Change PC008 from 0.47uF 0402 size (SE124474030) to 0.022uF 0402 size (SE075223030) Change FR054 from 100K 0402 size (SD034100080) to 84.5K 0402 size (SD034045030) Change FR057 from 25.4K 0402 size (SD034294280) to 15.4K 0402 size (SD034154280) Change FR051 from 4.97K 0402 size (SD034487100) to 10.5K 0402 size (SD034105280) Change FR055 from 21.5K 0402 size (SD034215280) to 18.2K 0402 size (SD034182280)	2017/11/13
8	38	Change main source (sourcing and Buyer requirements)	Change P02 from L2M70002DW (SE000000000) to L2M70002DW (SE000000000)	2017/11/16
9	48	Change CPU sequence (HW requirements)	Change PCW from 1u 0402 size (SE000000000) to 0.1u 0402 size (SE072104030)	2017/11/21
10	38,39,48	EMI requirements	Change PCB, FR012, PC15, PC11, PCW11, FR05, PCW0 unpop to pop Add PCW08 0.1u 0402 size 20V	2017/11/21
11	46	EMI requirements	Delete jump P10, Add head PLW (SE010000000)	2017/11/22

6L UMA X63AB982L02 X4PAB982L02  
8L M250 X63ABI32L02 X4PABI32L02

11	48	EMI requirements	Delete jump P10, Add head PLW (SE010000000)	2017/11/22
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Date: Wednesday, November 22, 2017		Sheet 50 of 50